DDR2 SDRAM tRFC Application Note

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MEMORY DIVISION

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Introduction

tRFC is an important memory timing parameter, necessary for the proper refresh of DRAM circuitry. This parameter is included in the industry-standard DRAM datasheet approved by JEDEC.

There are different tRFC minimum value specifications for each device density.

Insufficient tRFC will result in system failures, due to the occurrence of an incomplete refresh to the internal DRAM cells.

Samsung recommends that main-board and chipset suppliers check the tRFC values being used by their systems' BIOS against the requirements for the specific device densities being used.

Description of tRFC

Application Note

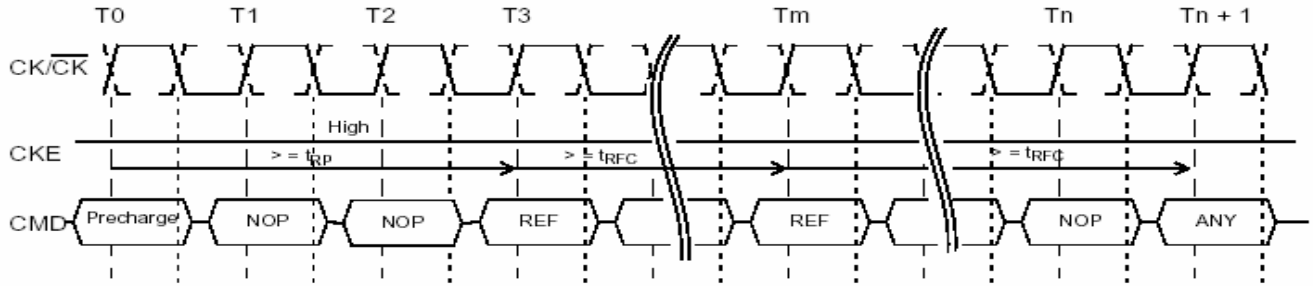
According to DDR2 SDRAM Specification in JEDEC and Samsung,

2.2.7 Refresh Command

When $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ are held low and $\overline{WE}$ high at the rising edge of the clock, the chip enters the Refresh mode (REF). All banks of the DDR2 SDRAM must be precharged and idle for a minimum of the Precharge time (tRP) before the Refresh command (REF) can be applied. An address counter, internal to the device, supplies the bank address during the refresh cycle. No control of the external address bus is required once this cycle has started.

When the refresh cycle has completed, all banks of the DDR2 SDRAM will be in the precharged (idle) state. A delay between the Refresh command (REF) and the next Activate command or subsequent Refresh command must be greater than or equal to the Refresh cycle time (tRFC).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight Refresh commands can be posted to any given DDR2 SDRAM, meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 9 * tREFI.

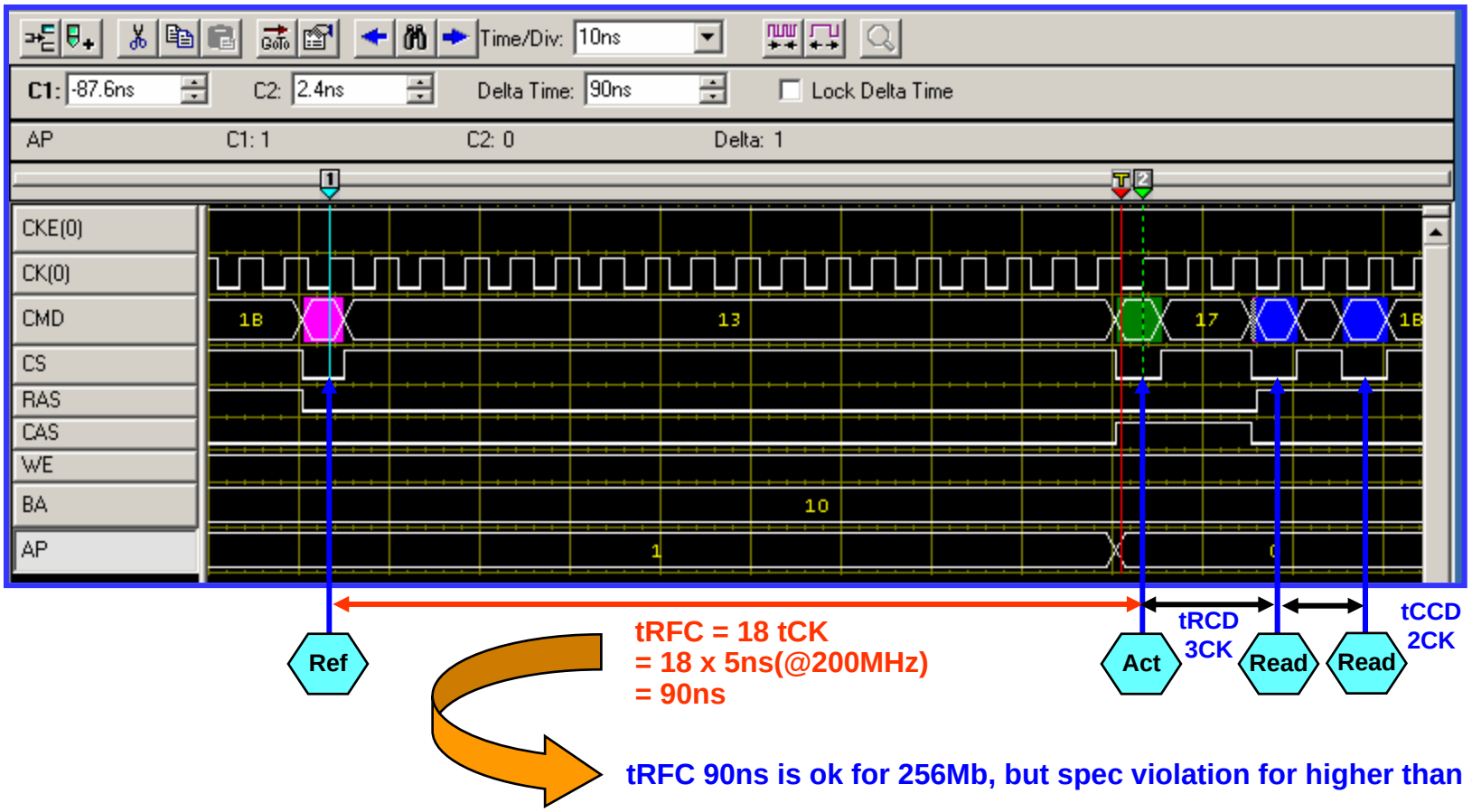


Refresh Parameters by Device Density

Parameter	Symbol		256Mb	512Mb	1Gb	2Gb	4Gb	Units
Refresh to active/Refresh command time	tRFC		75	105	127.5	195	327.5	ns
Average periodic refresh interval	tREFI	0 °C ≤ T_{CASE} ≤ 85°C	7.8	7.8	7.8	7.8	7.8	µs
		85 °C < T_{CASE} ≤ 95°C	3.9	3.9	3.9	3.9	3.9	µs

Example of tRFC timing @400Mbps

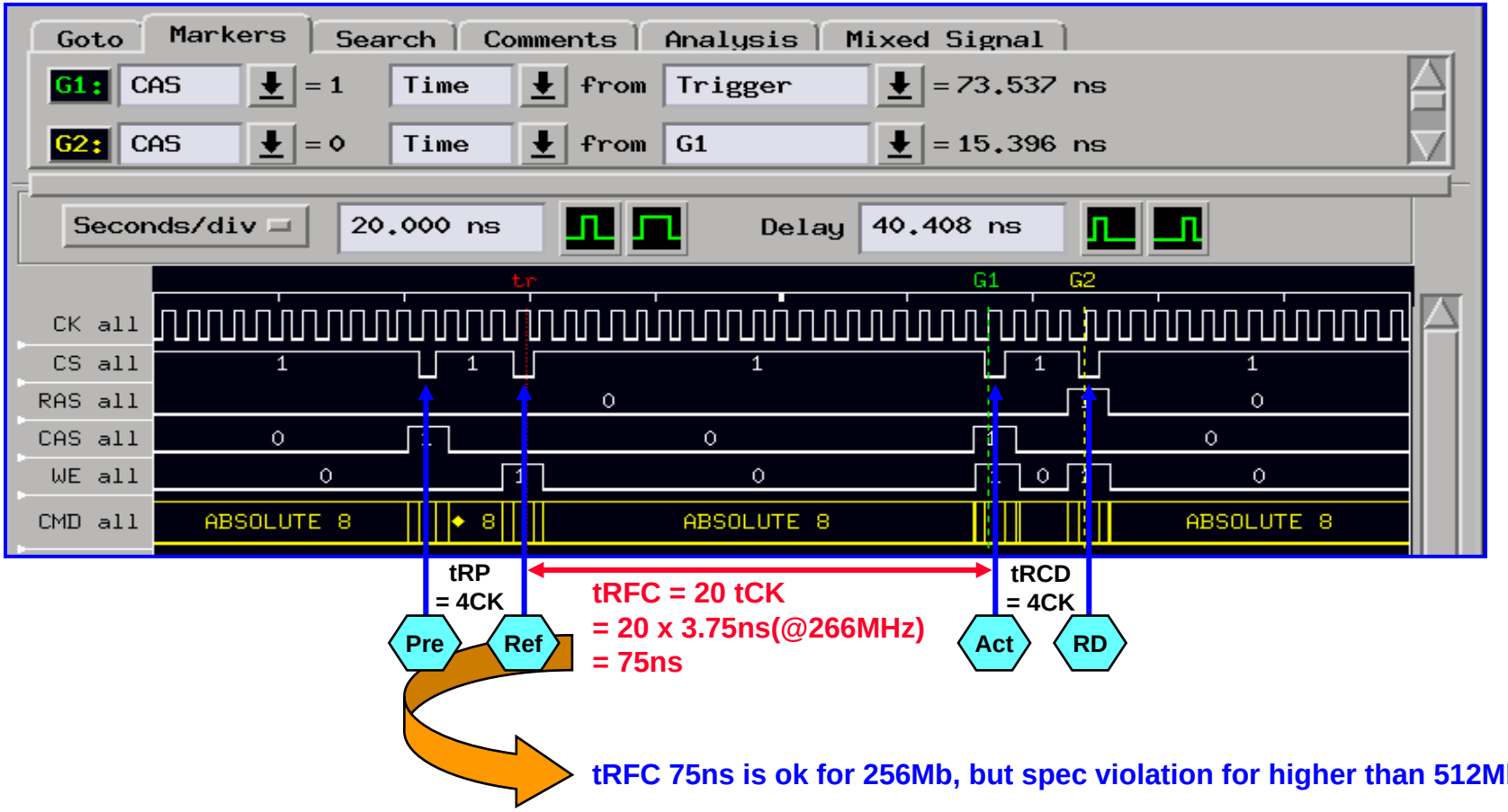
tRFC timing at DDR2-400 : CL-tRCD-tRP = 3-3-3 [CK]



For high density, 512Mb, 1Gb, 2Gb, and 4Gb DDR2 SDRAMs running @ 400Mbps, tRFC min. should be 21tCK (105ns), 26tCK (130ns), 39tCK (195ns), and 66tCK (330ns), respectively.

Example of tRFC timing @533Mbps

tRFC timing at DDR2-533 : CL-tRCD-tRP = 4-4-4 [CK]



tRFC 75ns is ok for 256Mb, but spec violation for higher than 512Mb.

For high density, 512Mb, 1Gb, 2Gb, and 4Gb DDR2 SDRAMs running @ 533Mbps, tRFC min. should be 28tCK (105ns), 34tCK (127.5ns), 52tCK (195ns), and 88tCK (330ns), respectively.

tRFC min. Table by Frequency & Density

tRFC minimum value by frequency & density for DDR2 SDRAM

	DDR2 Frequency	tCK	Device Density					unit
			256Mb	512Mb	1Gb	2Gb	4Gb	
	tRFC min. Specification		75	105	127.5	195	327.5	ns
Freq.	@400Mbps	5ns	15	21*	26*	39	66	Clock
	@533Mbps	3.75ns	20	28*	34*	52	88	Clock
	@667Mbps	3ns	25	35	43	65	110	Clock

*** Examples of tRFC calculations according to speed & device density**

for 512Mb device

@400Mbps : tCK x 21 Clock = 5ns x 21 = 105ns >= tRFC min. spec. = 105ns
@533Mbps : tCK x 28 Clock = 3.75ns x 28 = 105ns >= tRFC min. spec. = 105ns

for 1Gb device

@400Mbps : tCK x 21 Clock = 5ns x 26 = 130ns >= tRFC min. spec. = 127.5ns
@533Mbps : tCK x 28 Clock = 3.75ns x 34 = 127.5ns >= tRFC min. spec. = 127.5ns