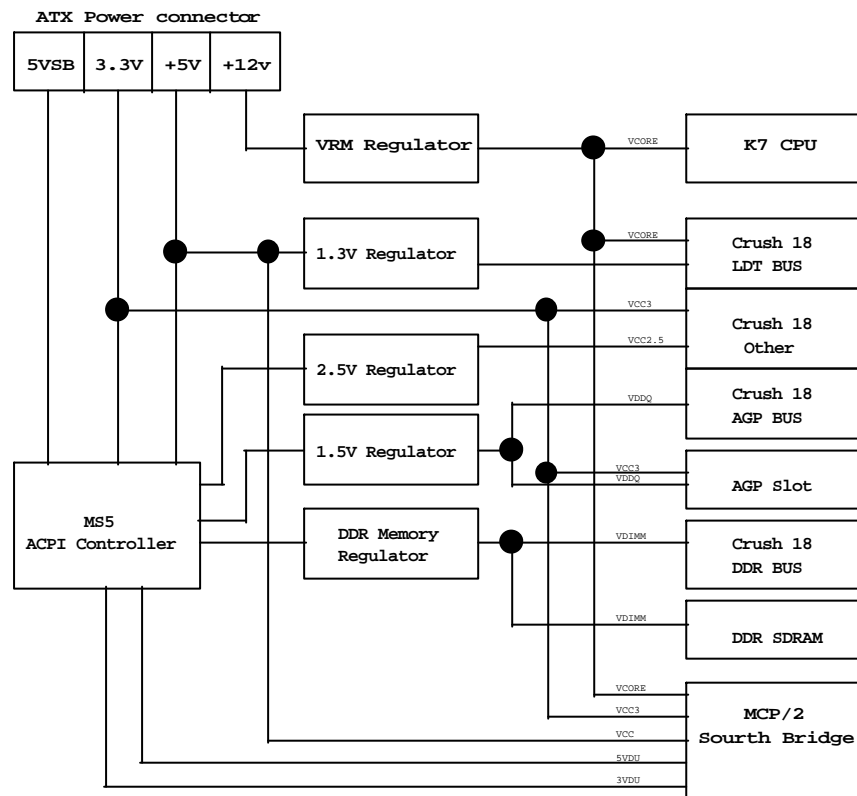


MS-6570 Version: 0B

Powered by
Venson.Chen

003-K7 CPU Part 1
004-K7 CPU Part 2
005-VRM 9.0
006-Crush17/18 Part 1
007-Crush17/18 Part 2
008-Crush17/18 Part 3
009-Crush17/18 Part 4
Power OK Circuit
010-AGP Slot & TV-out
011-DDR DIMM1 & 2
012-DDR DIMM3
013-DDR Terminator Resistor
014-MCP/2 Part 1
015-MCP/2 Part 2
016-MCP/2 Part 3
017-ACR Slot & MS3 & BIOS
018-MII LAN & USB Connector
019-IEEE1394 & VGA Connector
020-Realtek 650 AC97 codec
021-PCI Slot1 & 2
022-PCI Slot3 & 4
023-PCI Slot5 & MS1
024-On board Serial ATA
025-K/M Connector & IDE Connector
026-COM/Print Port
027-W83627HF LPC SIO & Game Port
028-MS5 ACPI Controller & Power
029-ATX Power & Front Panel
030-History

Title		
MS-6570		
Size	Document Number	Rev
	Blockdiagram	0A
Date: Thursday, August 01, 2002 Sheet: 1 of 30		



MS-6570 Specification

CPU: AMD K7 Serial Socket 462

North Bridge: Nvedia Crush 17/18

South Bridge: Nvidia MCP/2

On Board PCI Device: Serial ATA

On Board Device: RealTek AC97 Codec

On Board Device: IEEE1394 PHY

On Board Device: ICS MII LAN

On Board DDR SDRAM: X3

On Board AGP Slot: X1

On Board PCI Slot: X5

On Board ACR Slot: X1

GPIO and PCI BUS Address

CPU1A
PGA-D462

HSDATA#0	AA35	SDATA0
HSDATA#1	W37	SDATA1
HSDATA#2	W35	SDATA2
HSDATA#3	U35	SDATA3
HSDATA#4	U35	SDATA4
HSDATA#5	U33	SDATA5
HSDATA#6	S37	SDATA6
HSDATA#7	S33	SDATA7
HSDATA#8	AX33	SDATA8
HSDATA#9	AE37	SDATA9
HSDATA#10	AG33	SDATA10
HSDATA#11	AG37	SDATA11
HSDATA#12	Y37	SDATA12
HSDATA#13	AX37	SDATA13
HSDATA#14	AG35	SDATA14
HSDATA#15	S35	SDATA15
HSDATA#16	Q37	SDATA16
HSDATA#17	Q35	SDATA17
HSDATA#18	N37	SDATA18
HSDATA#19	J33	SDATA19
HSDATA#20	G33	SDATA20
HSDATA#21	G37	SDATA21
HSDATA#22	E37	SDATA22
HSDATA#23	G35	SDATA23
HSDATA#24	Q33	SDATA24
HSDATA#25	N33	SDATA25
HSDATA#26	L33	SDATA26
HSDATA#27	N35	SDATA27
HSDATA#28	L37	SDATA28
HSDATA#29	L37	SDATA29
HSDATA#30	A37	SDATA30
HSDATA#31	E35	SDATA31
HSDATA#32	E31	SDATA32
HSDATA#33	E29	SDATA33
HSDATA#34	A27	SDATA34
HSDATA#35	A25	SDATA35
HSDATA#36	E21	SDATA36
HSDATA#37	C23	SDATA37
HSDATA#38	C27	SDATA38
HSDATA#39	A23	SDATA39
HSDATA#40	A35	SDATA40
HSDATA#41	C35	SDATA41
HSDATA#42	C33	SDATA42
HSDATA#43	C31	SDATA43
HSDATA#44	A29	SDATA44
HSDATA#45	C29	SDATA45
HSDATA#46	E23	SDATA46
HSDATA#47	C25	SDATA47
HSDATA#48	E17	SDATA48
HSDATA#49	E13	SDATA49
HSDATA#50	E11	SDATA50
HSDATA#51	E15	SDATA51
HSDATA#52	E9	SDATA52
HSDATA#53	A13	SDATA53
HSDATA#54	C9	SDATA54
HSDATA#55	A9	SDATA55
HSDATA#56	C21	SDATA56
HSDATA#57	A21	SDATA57
HSDATA#58	E19	SDATA58
HSDATA#59	C19	SDATA59
HSDATA#60	C17	SDATA60
HSDATA#61	A11	SDATA61
HSDATA#62	A17	SDATA62
HSDATA#63	A15	SDATA63

HSDINCLK#0	W33	SDATAINCLK0
HSDINCLK#1	J35	SDATAINCLK1
HSDINCLK#2	E27	SDATAINCLK2
HSDINCLK#3	E15	SDATAINCLK3

6 HSDINVAL# << HSDINVAL# AN33 SDATAINVAL#

6 HSDOUTCLK#0 << HSDOUTCLK#0 AE35 SDATAOUTCLK0

6 HSDOUTCLK#1 << HSDOUTCLK#1 G37 SDATAOUTCLK1

6 HSDOUTCLK#2 << HSDOUTCLK#2 A33 SDATAOUTCLK2

6 HSDOUTCLK#3 << HSDOUTCLK#3 C11 SDATAOUTCLK3

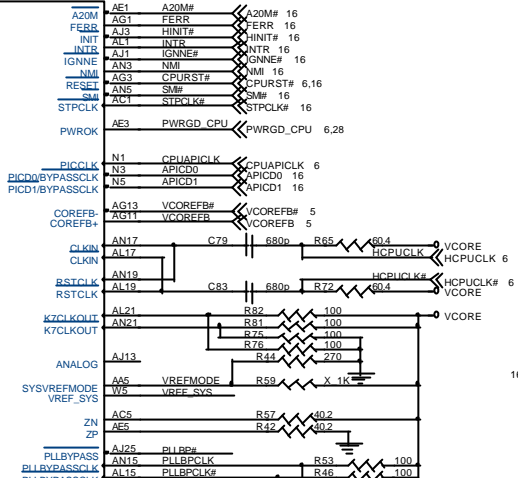
HSDOUTVAL#	AL31	SDATOUTVAL
HSDIN#0	AJ29	SADDIN0
HSDIN#1	AJ29	SADDIN1
HSDIN#2	AG33	SADDIN2
HSDIN#3	AJ37	SADDIN3
HSDIN#4	AL35	SADDIN4
HSDIN#5	AE33	SADDIN5
HSDIN#6	AJ35	SADDIN6
HSDIN#7	AG37	SADDIN7
HSDIN#8	AJ33	SADDIN8
HSDIN#9	AN37	SADDIN9
HSDIN#10	AL37	SADDIN10
HSDIN#11	AG35	SADDIN11
HSDIN#12	AN29	SADDIN12
HSDIN#13	AN35	SADDIN13
HSDIN#14	AN31	SADDIN14
HSDINCLK#	AJ33	SADDINCLK

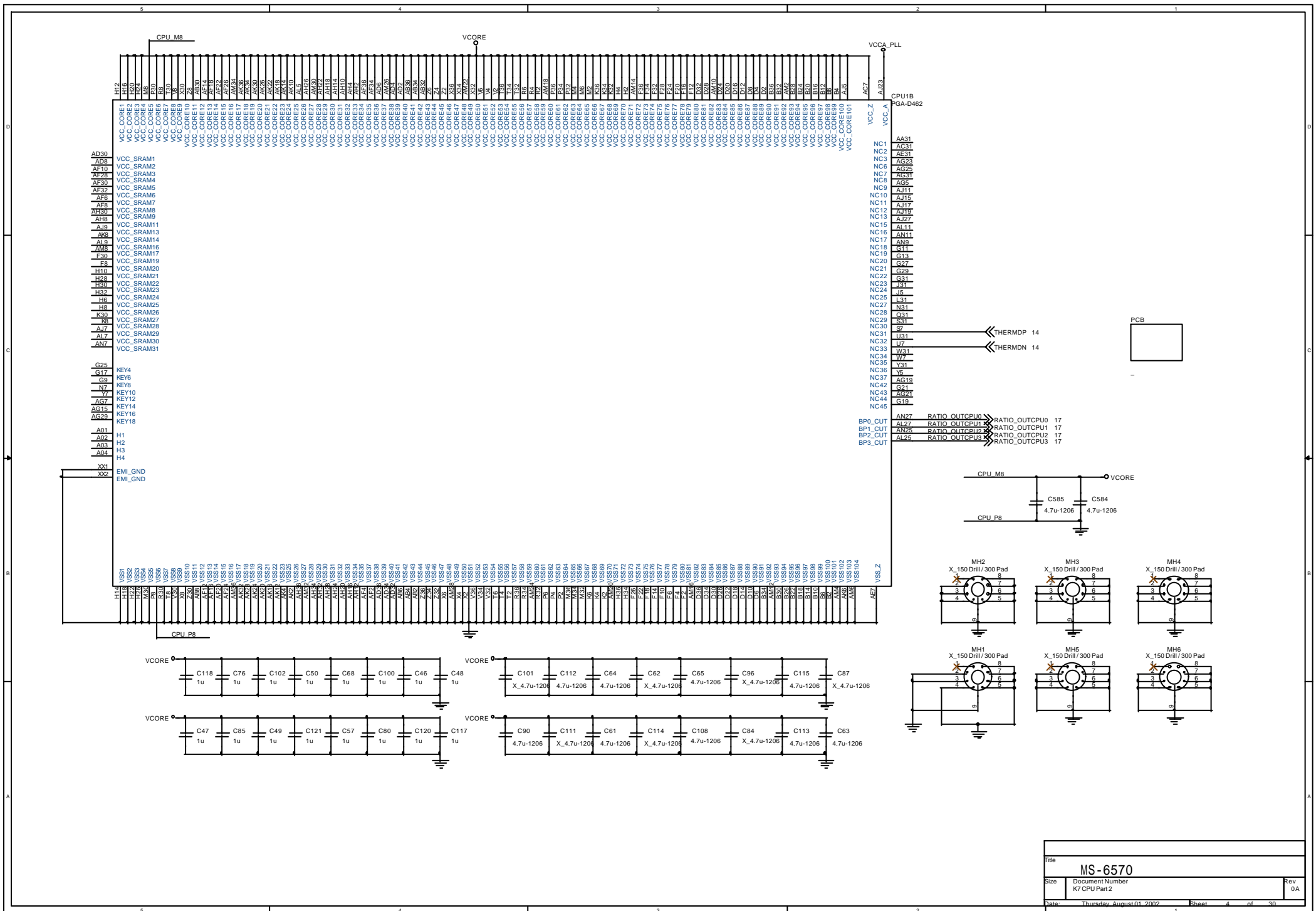
6 CLKFWDRST << CLKFWDRST AJ21 CLKFWDRST

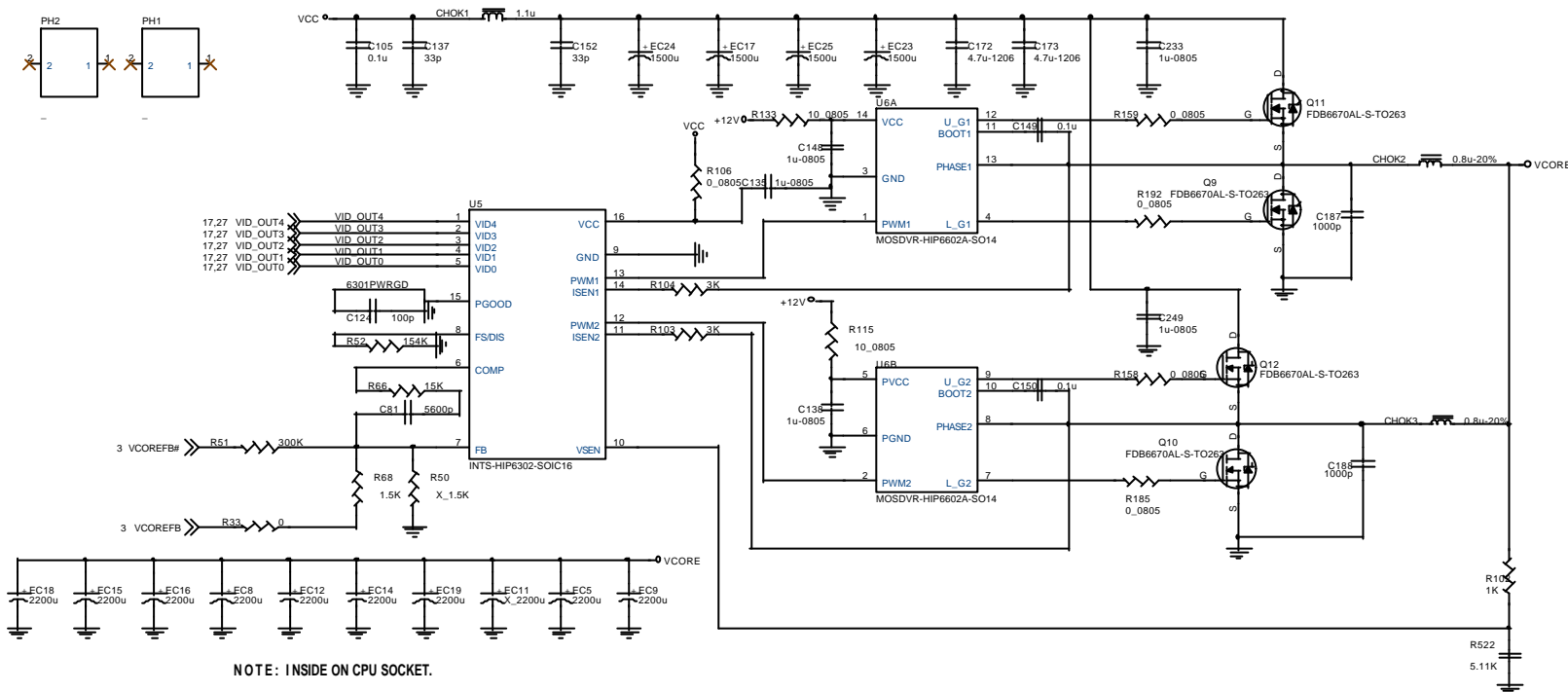
6 CONNECT << CONNECT AJ23 CONNECT

6 PROCRDY << PROCRDY AN23 PROCRDY

6 SFILLVAL# << SFILLVAL# AJ31 SFILLVAL#







VID4	VID3	VID2	VID1	VID0
VCC(V)	0	1	1	0
1.30	0	0	0	1
1.425	0	0	0	0
0.45	1	1	1	1
0.475	1	1	1	0
0.500	1	1	0	1
0.525	1	1	0	0
0.550	1	0	1	1
0.575	1	0	1	0
0.600	1	0	0	1
1.625				

VID4	VID3	VID2	VID1	VID0
VCC(V)	1	0	0	0
0.650	0	1	1	1
0.675	0	1	1	0
0.700	0	1	0	1
0.725	0	1	0	0
0.750	0	0	1	1
0.775	0	0	1	0
0.800	0	0	0	1
0.825	0	0	0	0
1.85	1	1	1	1
OFF				

FDB6670 Specification:

Qg= 35nC; Trise= 15ns; Tfall= 42ns

Hi-Side MOSFET:

Switching loss=

$$1/2 * I_o * V_{in} * (Trise + Tfall) * F_s$$

$$1/2 * 22.5 * 5 * (15ns + 42ns) * 200K$$

$$P_{switching loss} = 0.64W$$

$$Conduction loss = I_o^2 * R_{ds(on)} * D$$

$$= (22.5 * 22.5) * 0.0065 * 0.33 = 1.1W$$

$$P_{total} = P_{switching loss} + P_{conduction loss}$$

$$= 0.64W + 1.1W = 1.74W$$

Low-Side MOSFET:

$$P_{total} = (22.5 * 22.5) * 0.0065 * 0.67$$

$$= 2.2W$$

AMD CPU specification:

2GHz CPU: Vcore= 1.65V, P= 74.1W

Vcore_DC= -50mV ~ 50mV

Vcore_AC= -100mV ~ 150mV

$$I_{ripple} = I_o \sqrt{D(1-D)}$$

$$D = 1.65/5 = 33\%; I_{ripple} = 10.58A$$

The ripple current for each input

Based on temperature coefficient of Rubycon:

ripple current temperature coefficient temperature

2.55A 1 105

4.3A 1.7 85

5.4A 2.1 under 65

Total 4 pcs input capacitance= 17.2A @85

$$ESR = V_o(\Delta) / I_o(\Delta)$$

$$ESR = 100mV / 45 = 2.22m_{ohm}$$

ESR for each capacitance is 13m_ohm

Total 10 pcs capacitance are 1.3 m_ohm

1.3 m_ohm < 2.2 m_ohm, so it OK !

Rubycon 2200uF/6.3V capacitor

Rated voltage: 6.3V

Surge voltage: 8V

Leakage current: 415uA/2min

DF= 0.24@120Hz

Ripple current= 2.55A(max)

Vender guaranteed: 3000 Hr/105 degree.C

Actual operating temperature: 55 degree.C @45A

Ambient temperature: 25 degree.C

$$\text{實際壽命} = L1 * 2^{[(T1-Ta)/10]} * 2^{[(Ta-T2)/K]}$$

K= 10, if ripple current within specification

K= 5, if ripple current over specification

$$\text{實際壽命} = L1 * 2^{[(T1-T2)/10]}$$

$$\text{實際壽命} = 3000 * 2^{[(105-55)/10]}$$

$$\text{實際壽命} = 96000 \text{ Hr}$$

Ripple current of Vender's design:

$$I_{ac} =$$

$$\frac{\Delta(T) * B * A * WC}{\tan G}$$

Delta(T): 溫升 ; A= 0.785*{[D(D+4L)]/10}

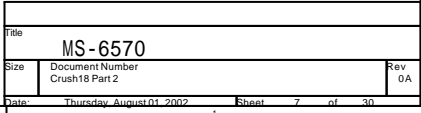
B: 散熱係數 ; WC= 6.28*E*C

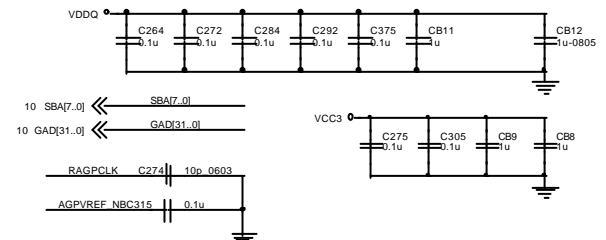
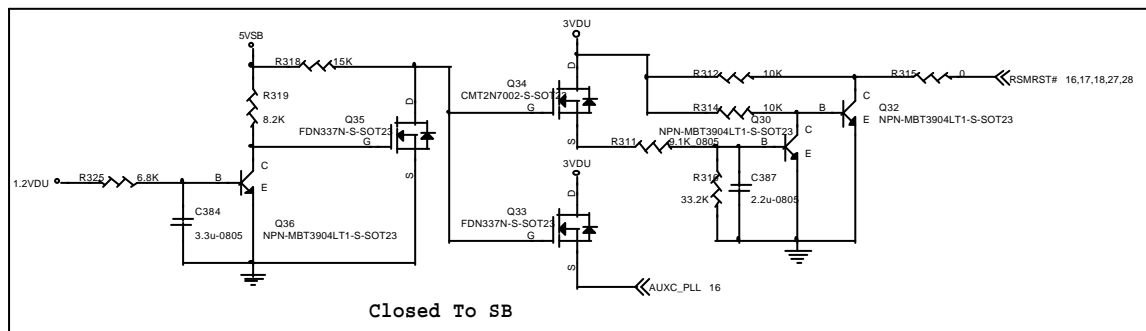
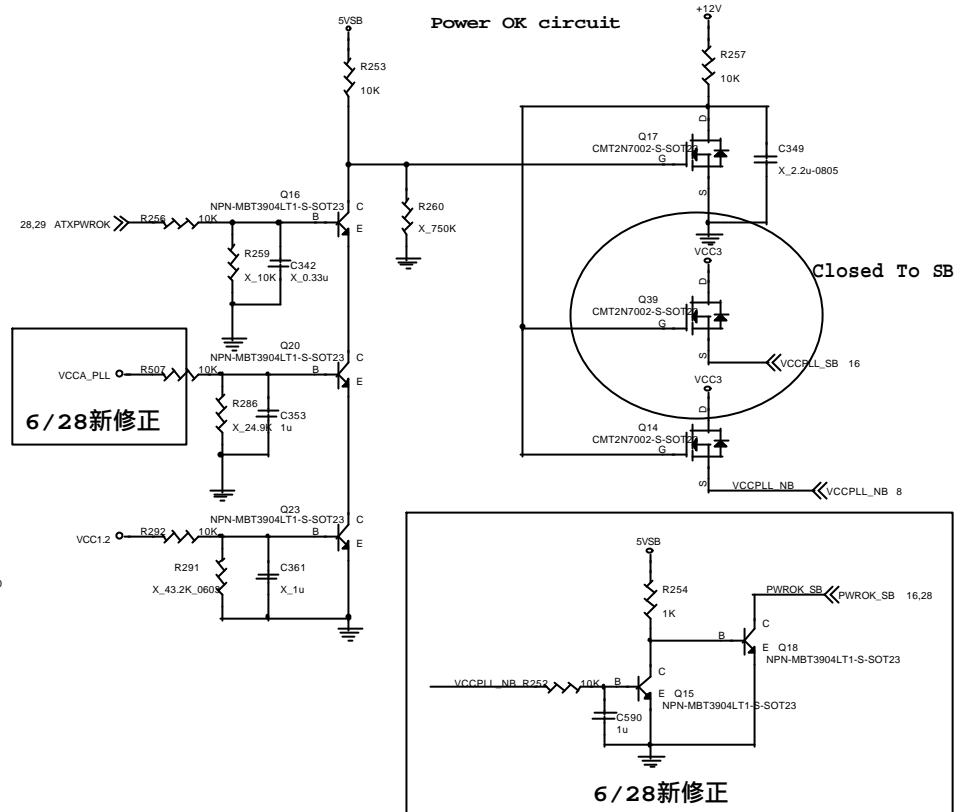
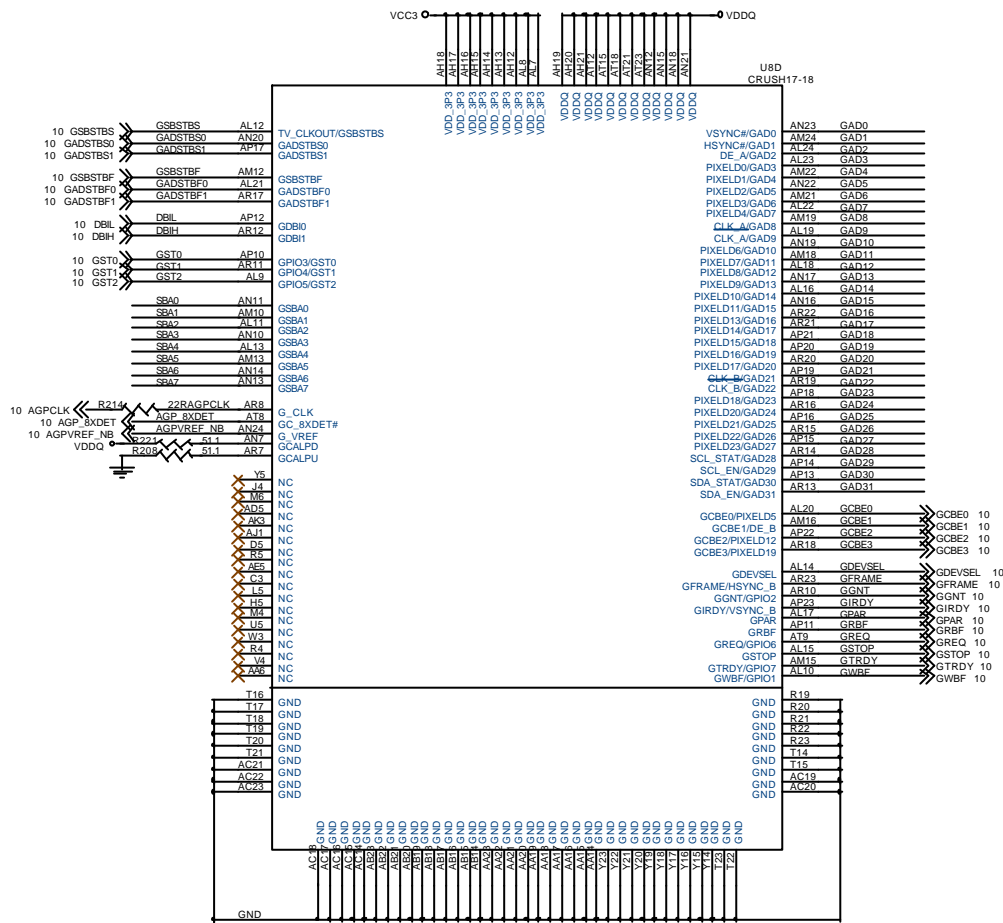
D: 電容外徑 ; L: 電容長度

$$\tan G = R/Xc ;$$

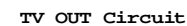
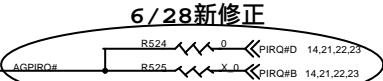
$$DF(\text{電容損失角}) = \tan G * 100\%$$

Title		
MS-6570		
Size	Document Number	Rev
VPM9.0		0A
Date	Thursday, August 01, 2002	Sheet 5 of 30

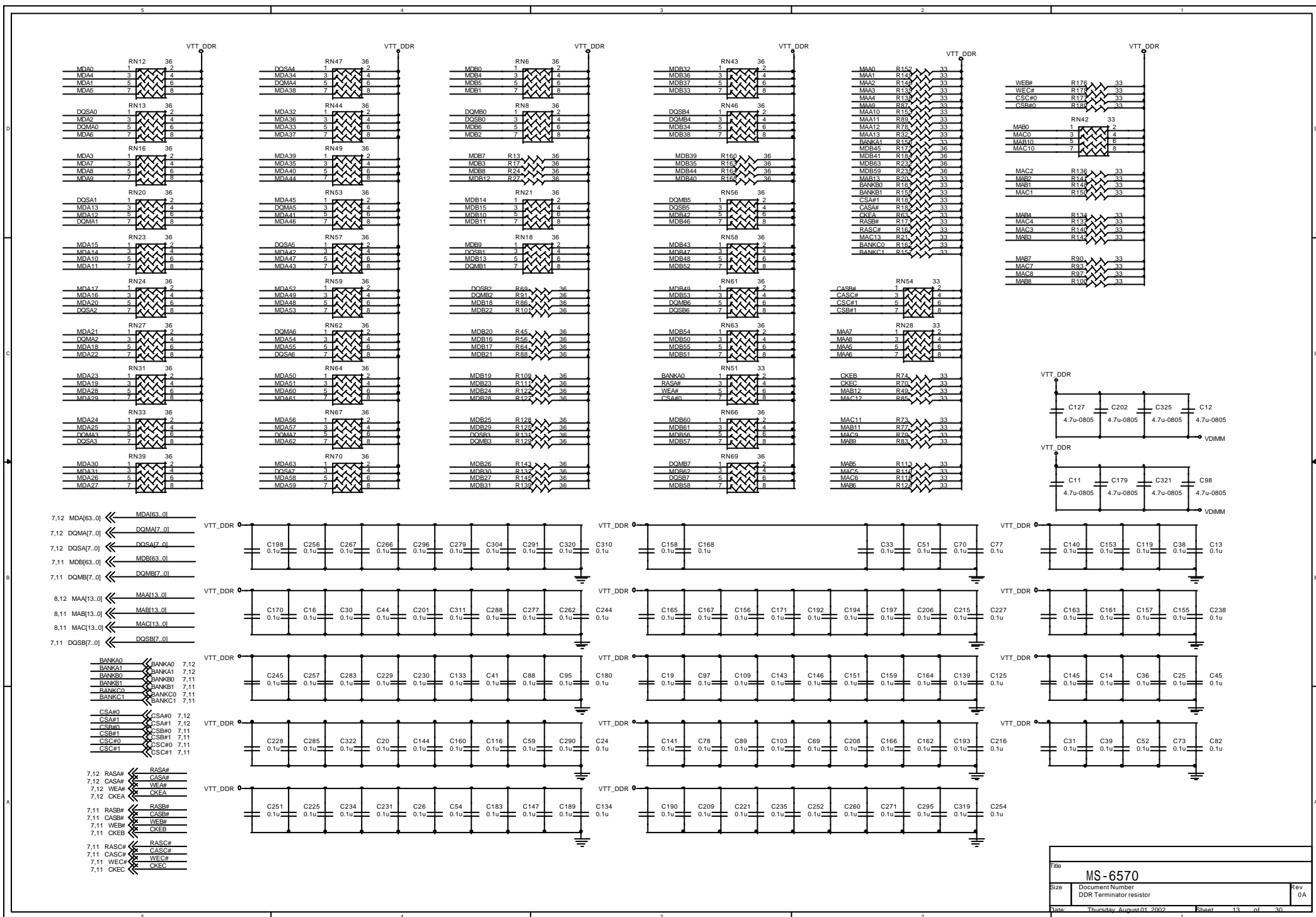


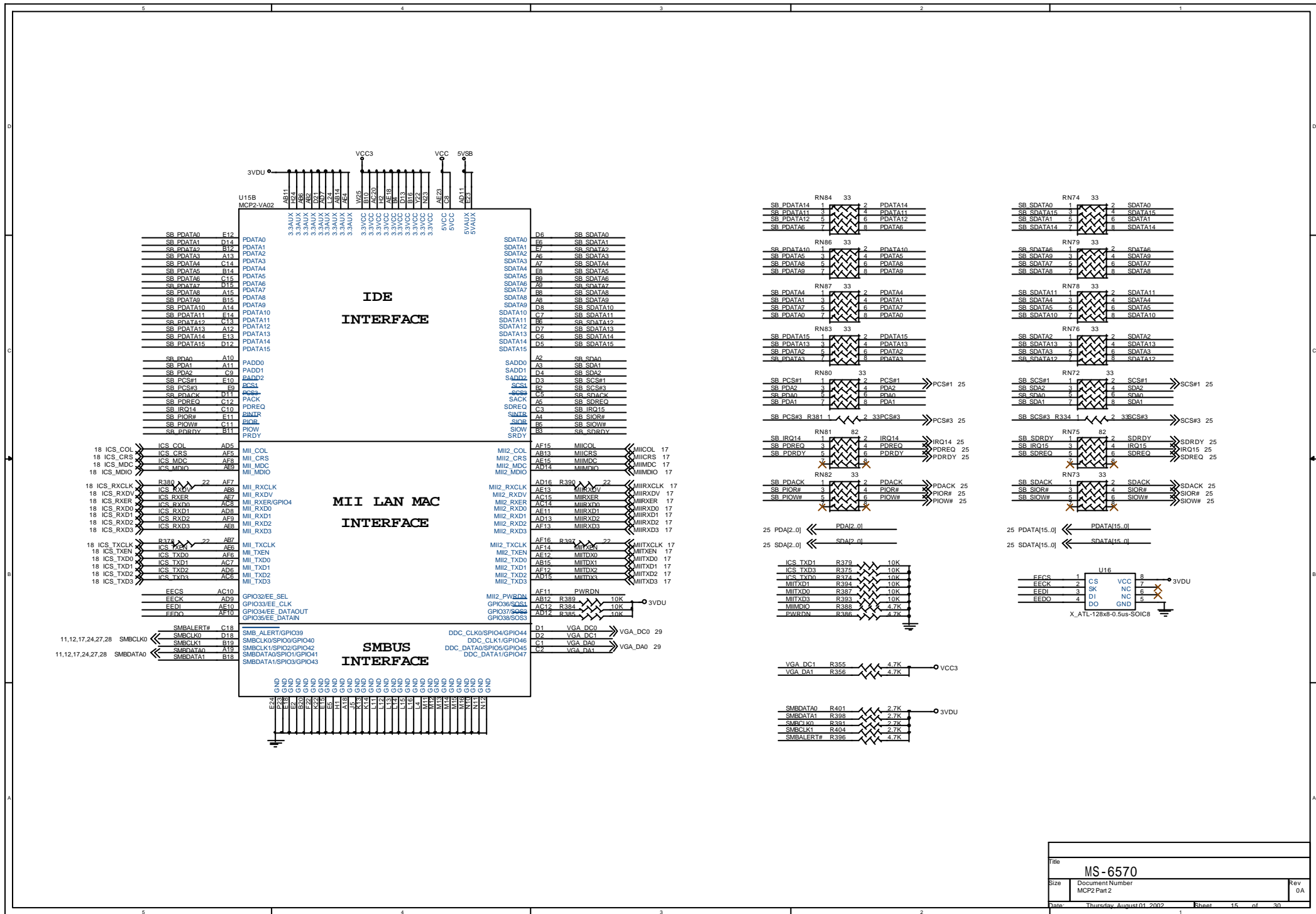


Title			MS-6570
Size	Document Number	Rev	0A
Crush18 Part 4			
Date	Thursday, August 01, 2002	Sheet	9 of 30

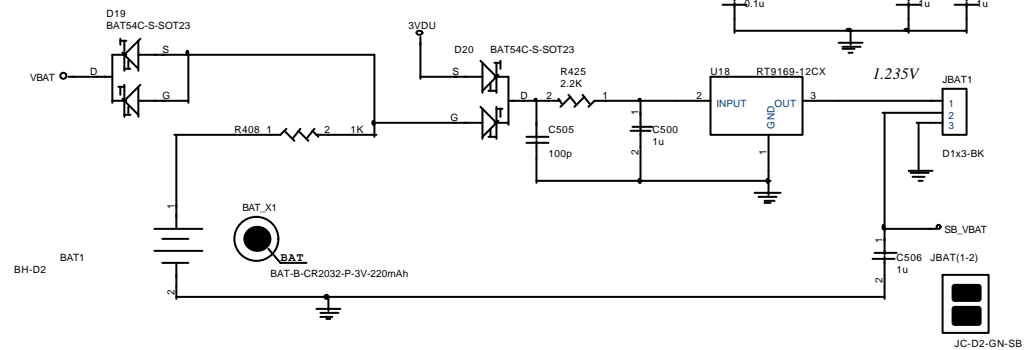
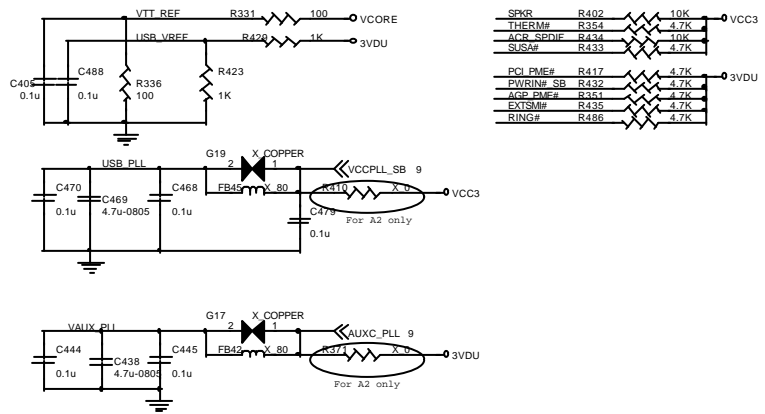
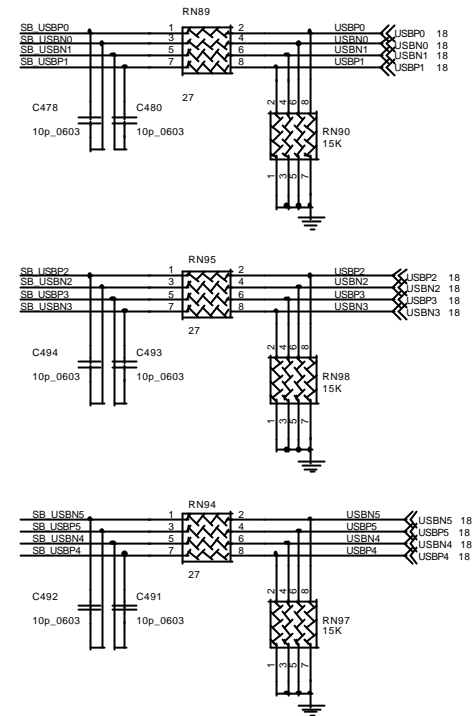
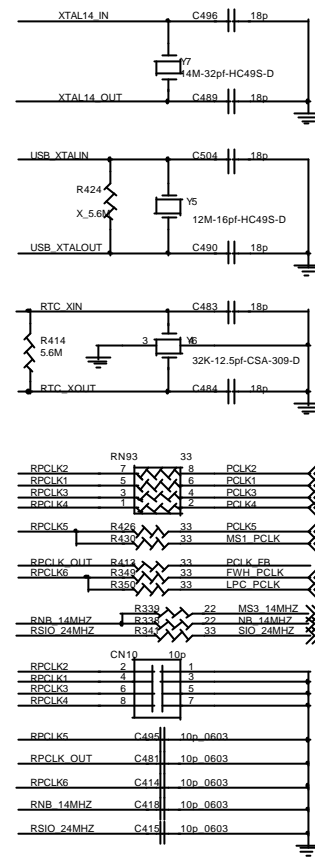
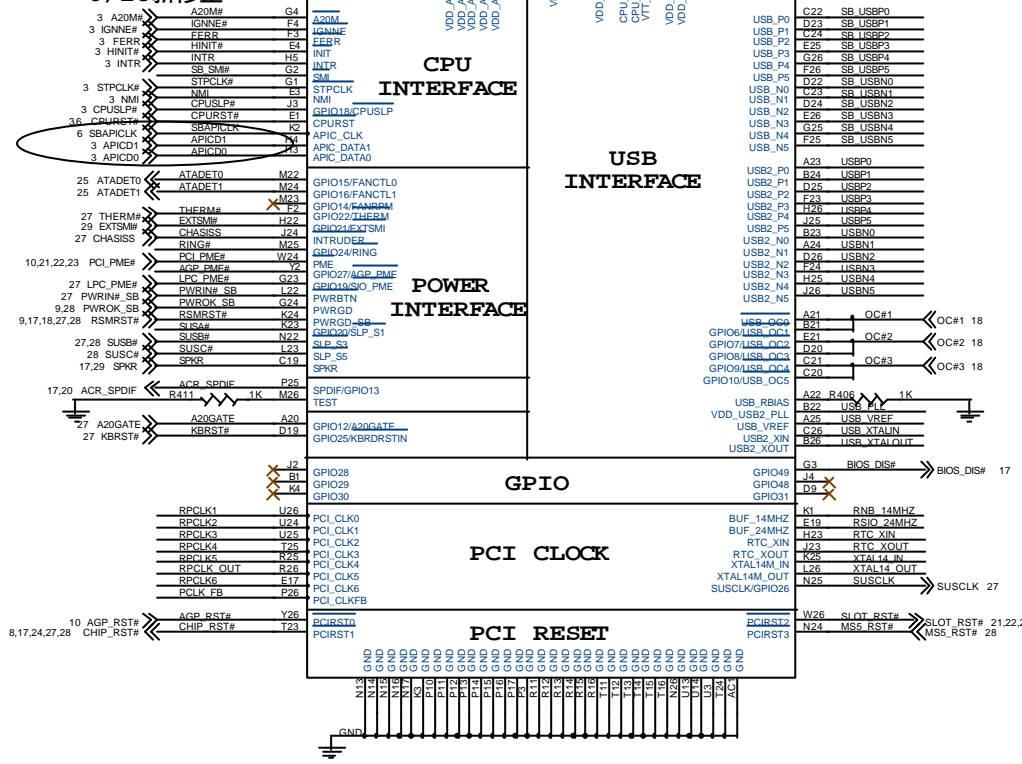


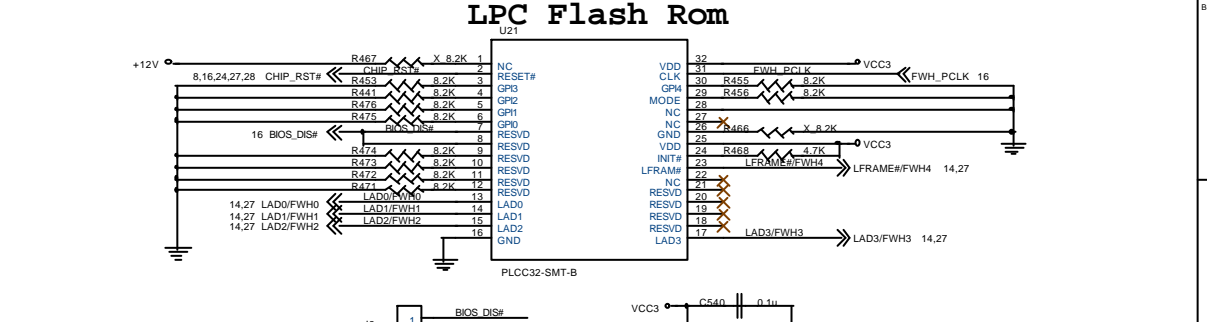
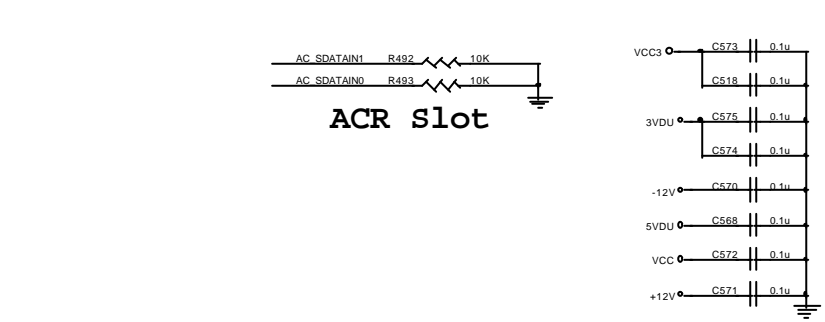
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MS-6570			
Size	Document Number AGP Slot 1.5V		Rev 01
Date	Thursday, August 01, 2002		Sheet 10 of 30

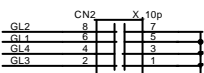
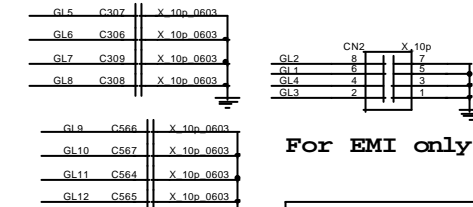
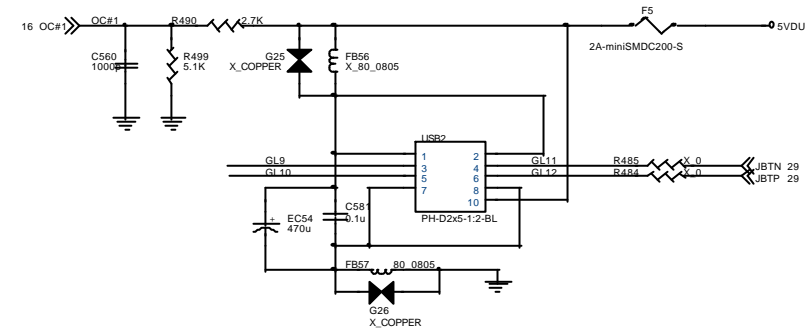
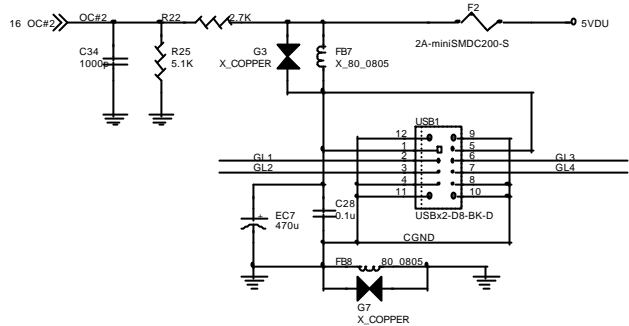
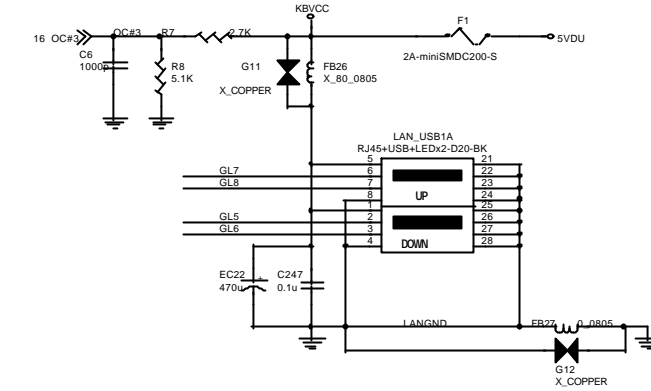
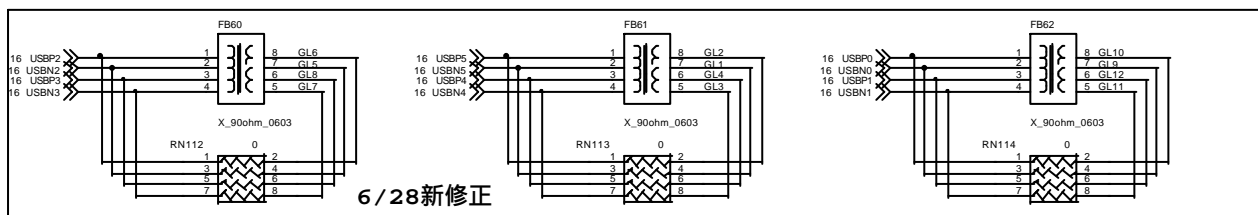
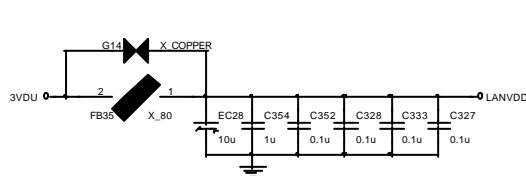
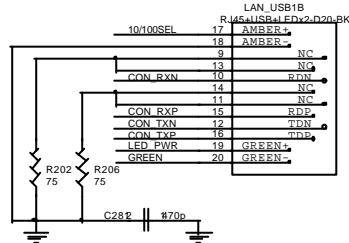
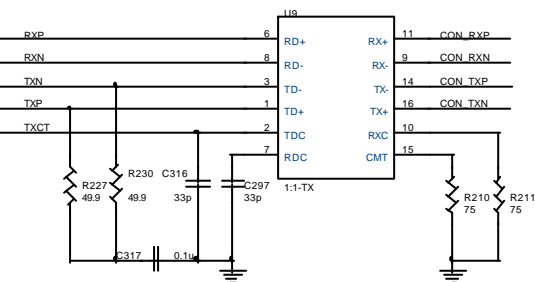
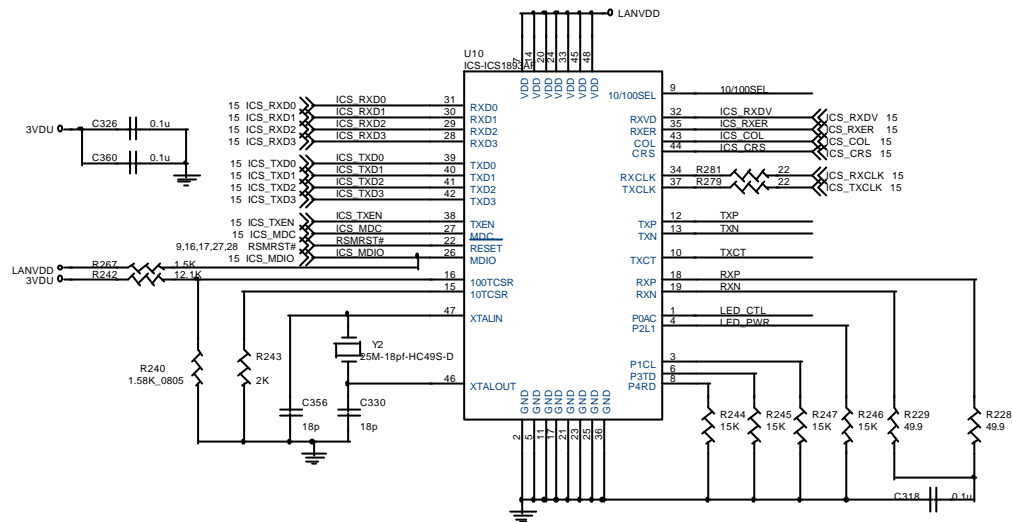




6/28新修正

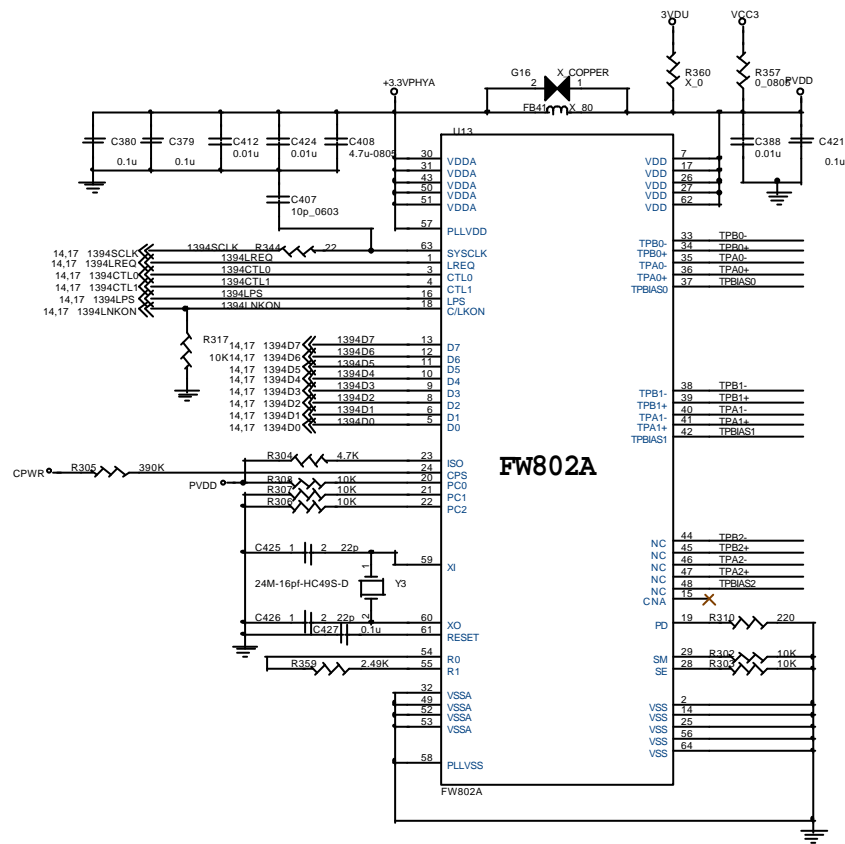




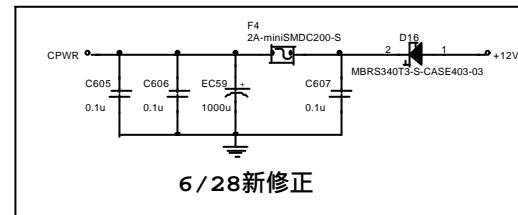
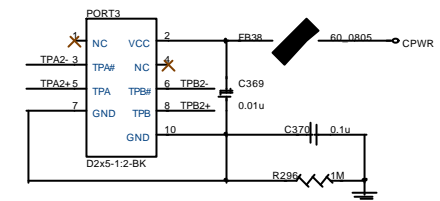
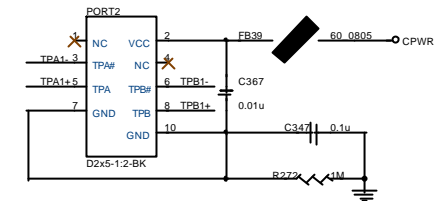
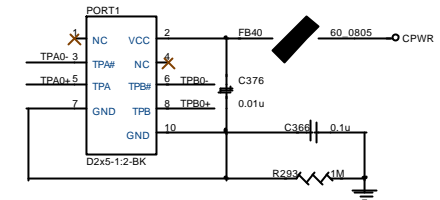
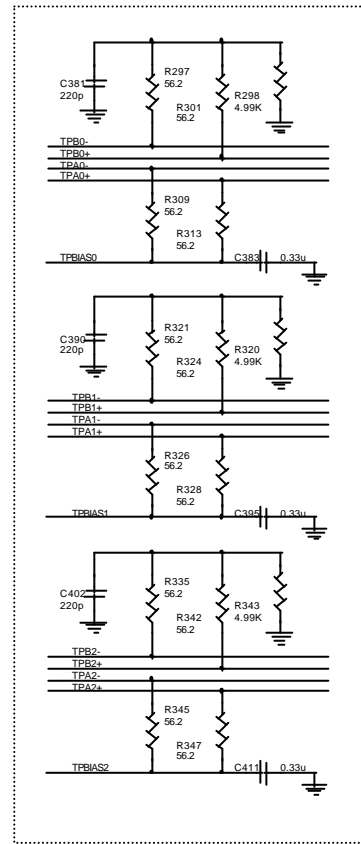


For EMI only

Title		MS-6570
Size	Document Number	Rev 0A
Date		Thursday, August 01, 2002
Sheet		18 of 30

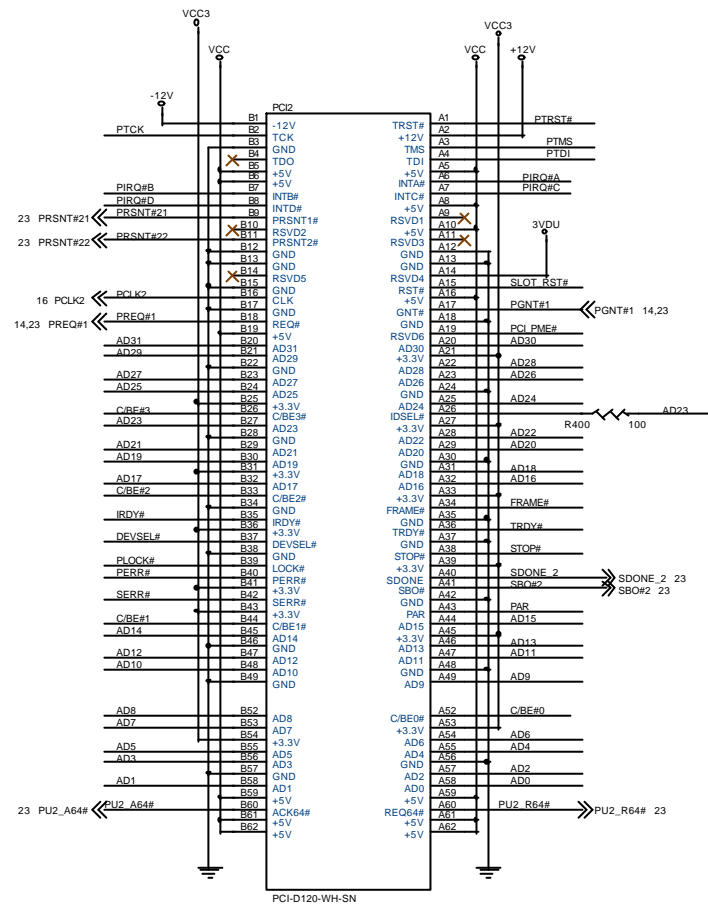
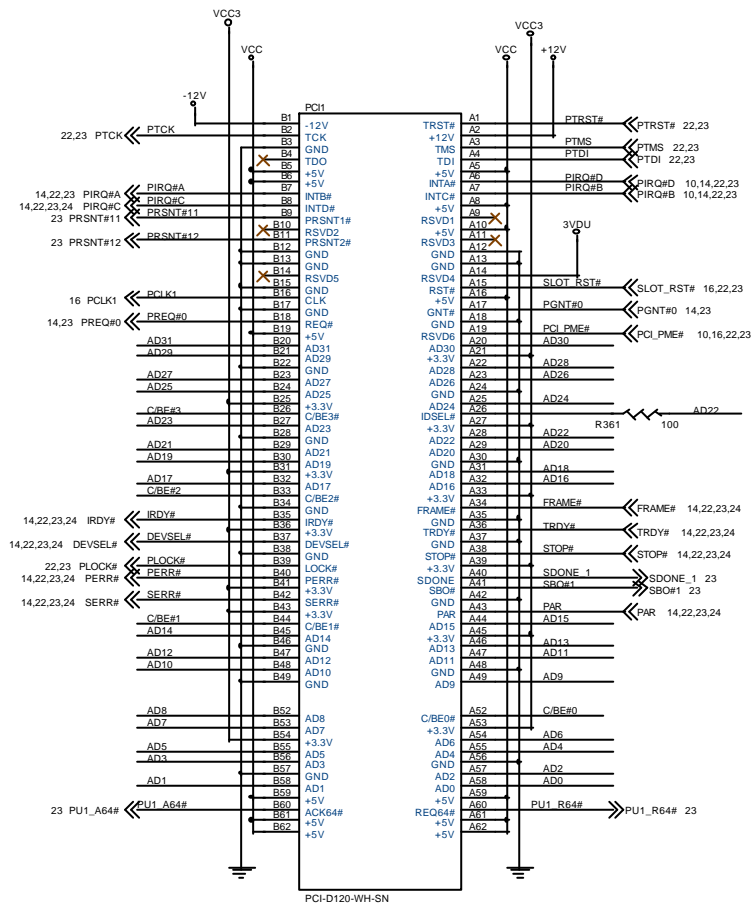


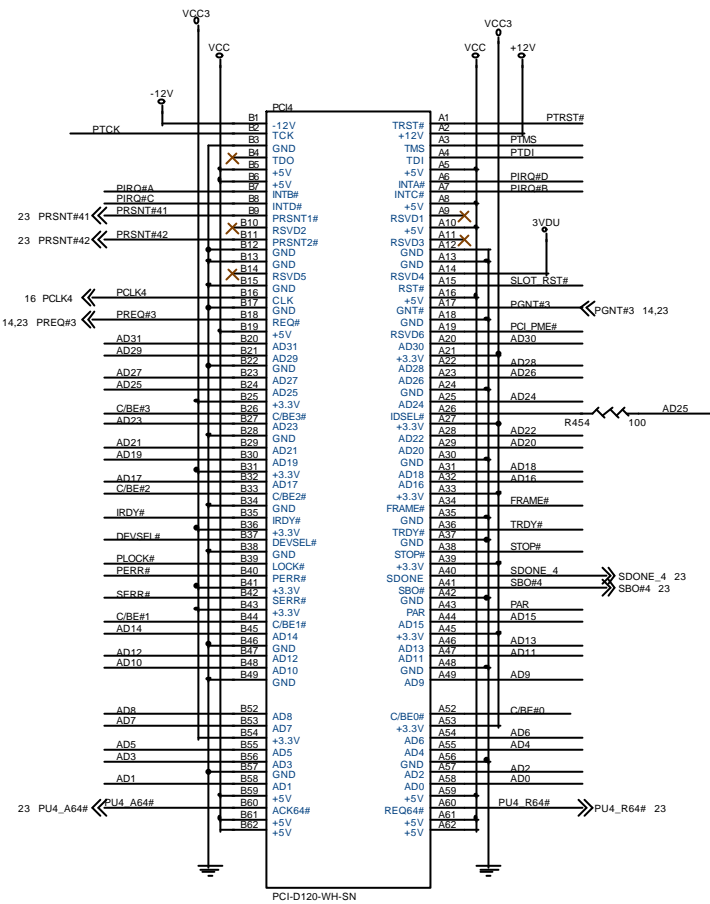
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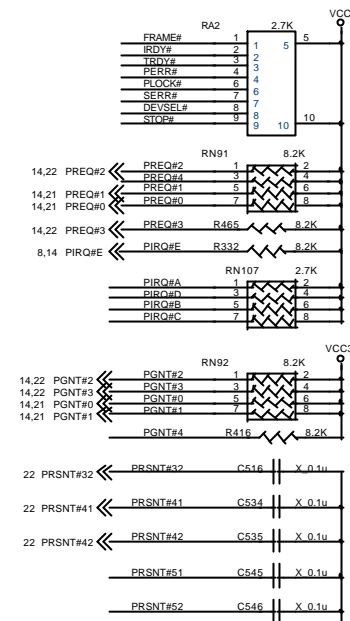
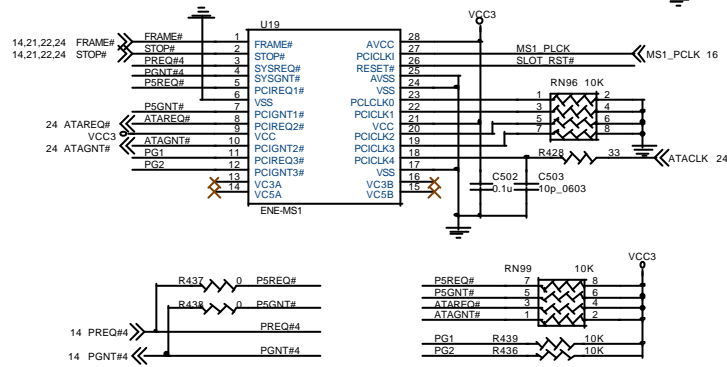
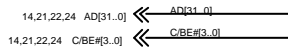


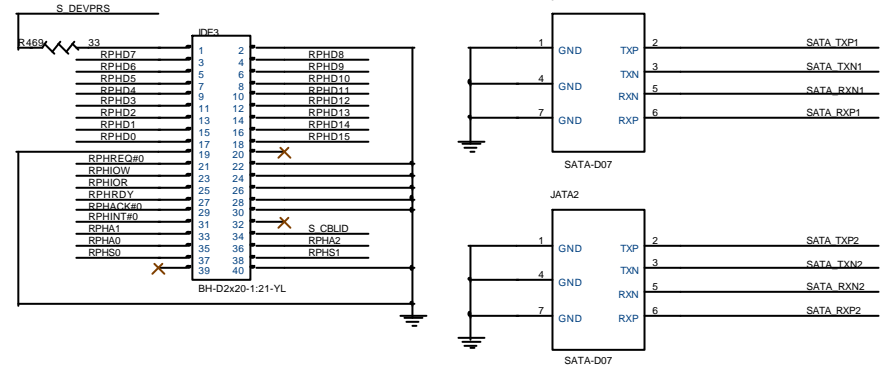
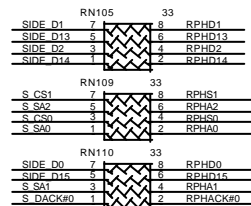
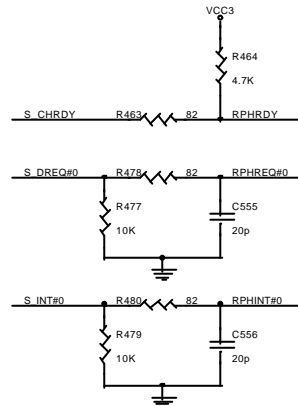
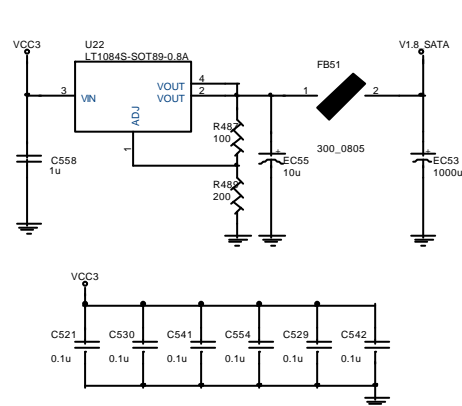
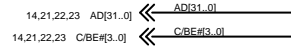
6/28新修正

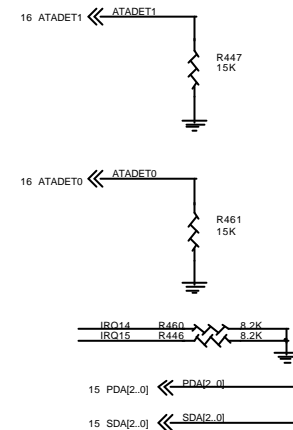
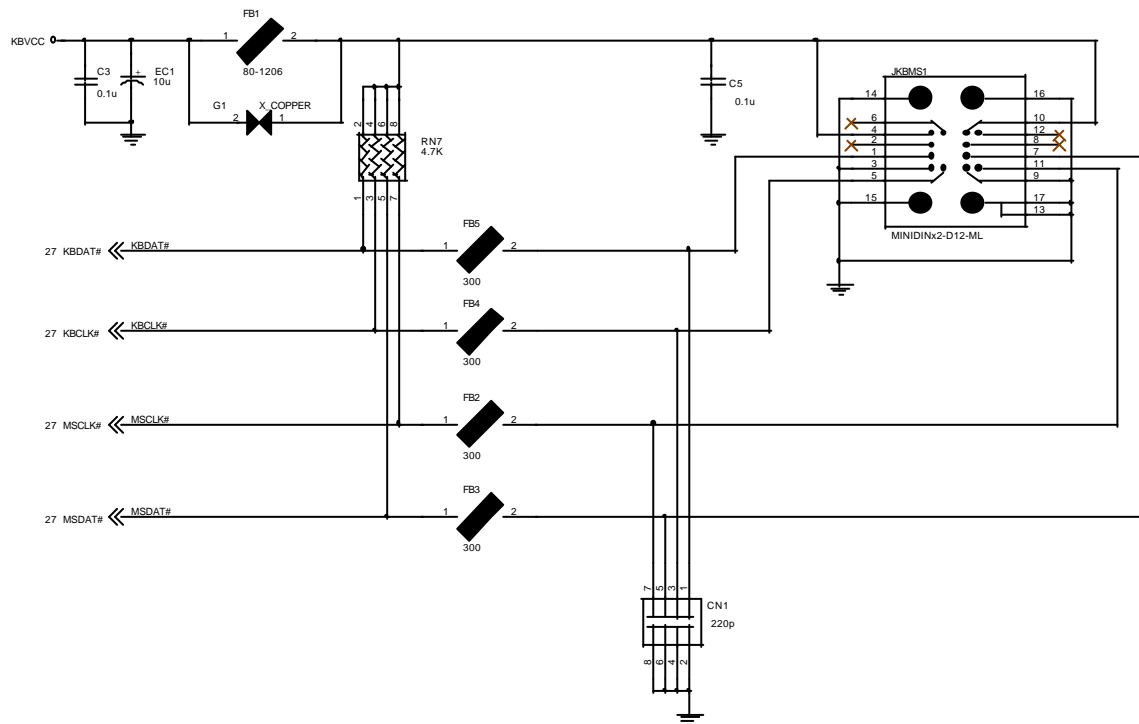
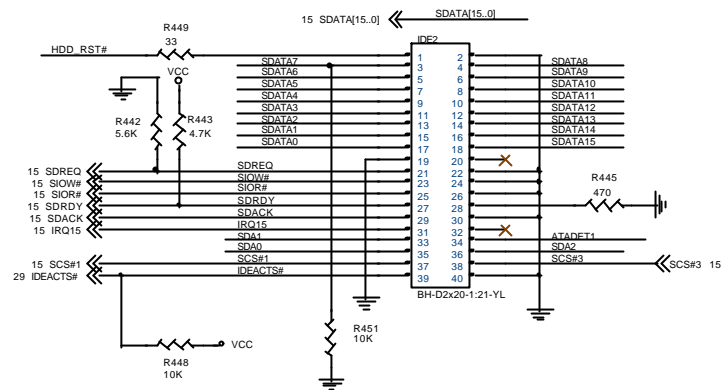
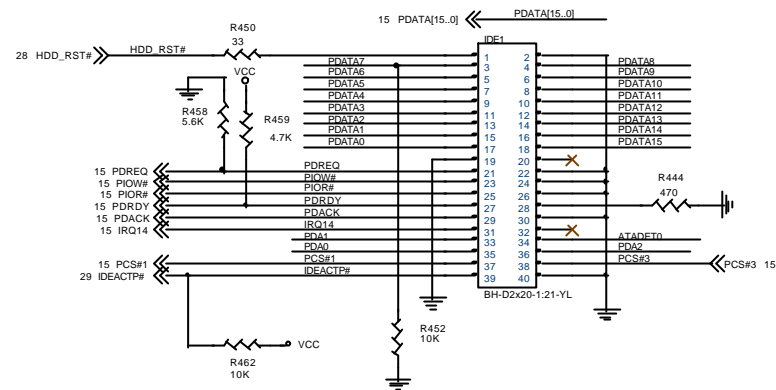
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MS-6570		
Size	Document Number	Rev
1394 PHY		0A
Date	Thursday, August 01, 2002	Sheet 18 of 30

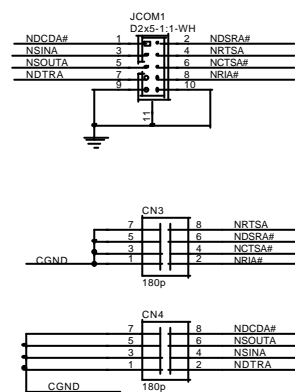
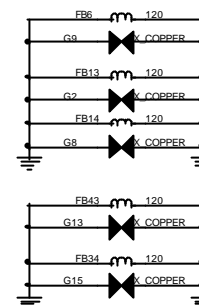
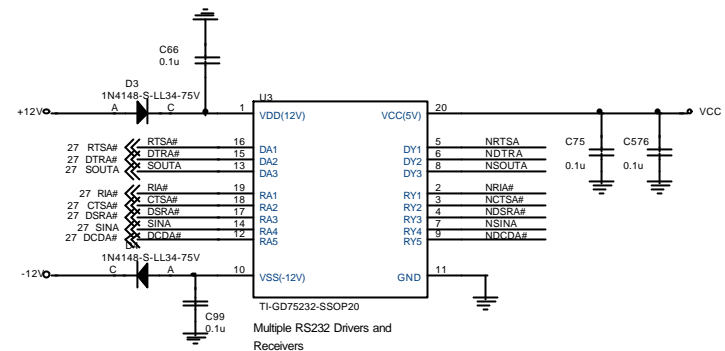


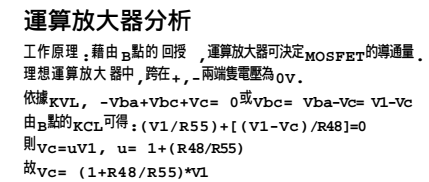
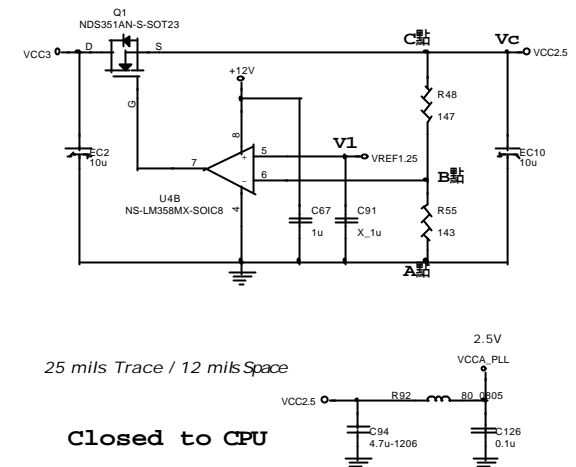






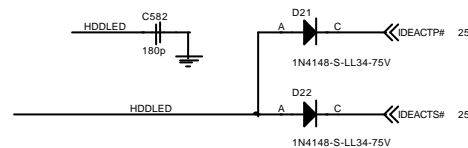




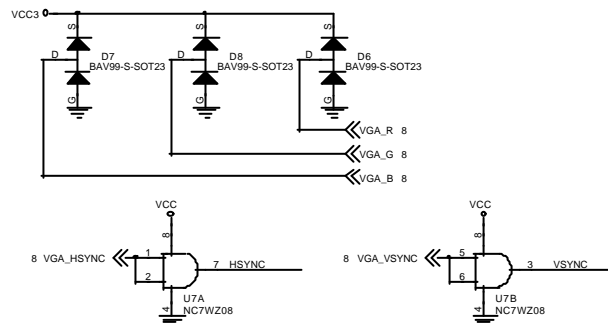
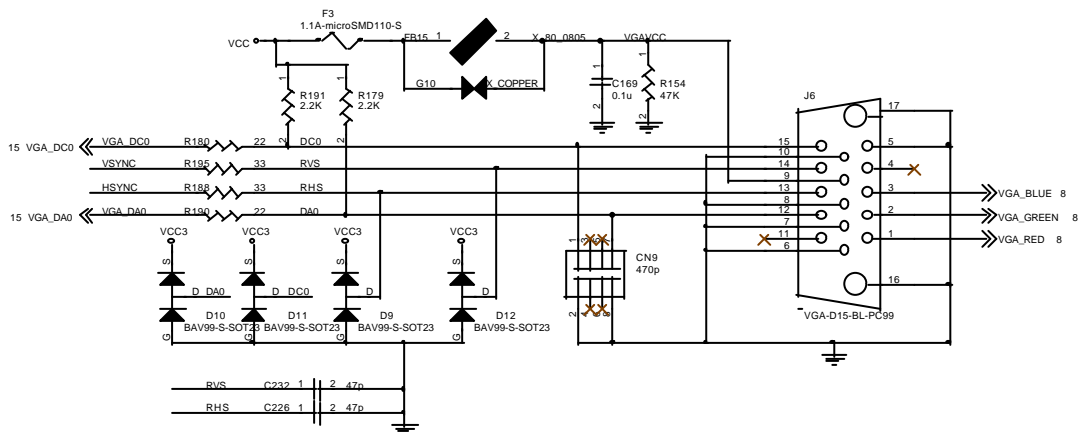
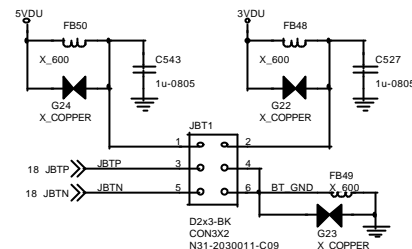
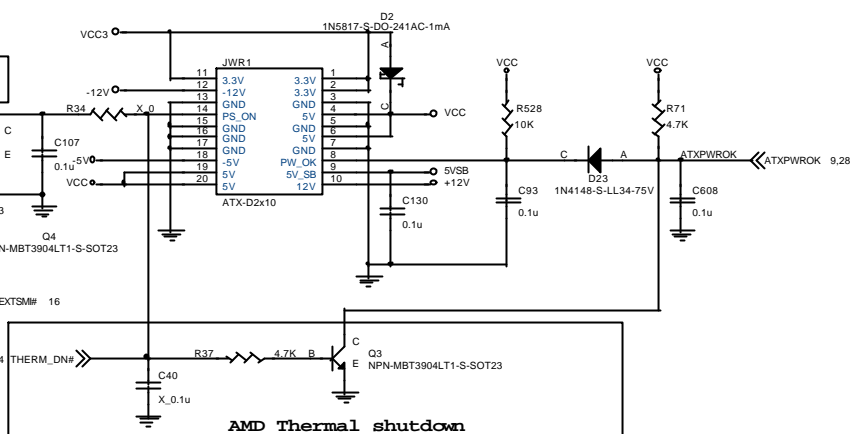
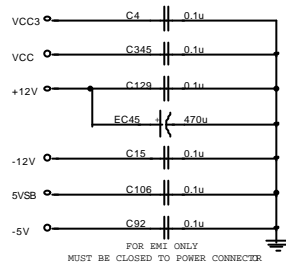
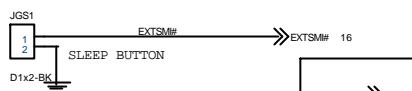
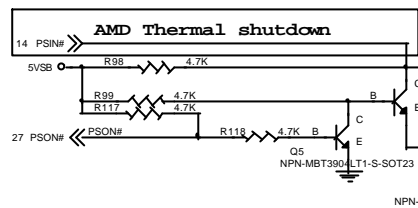
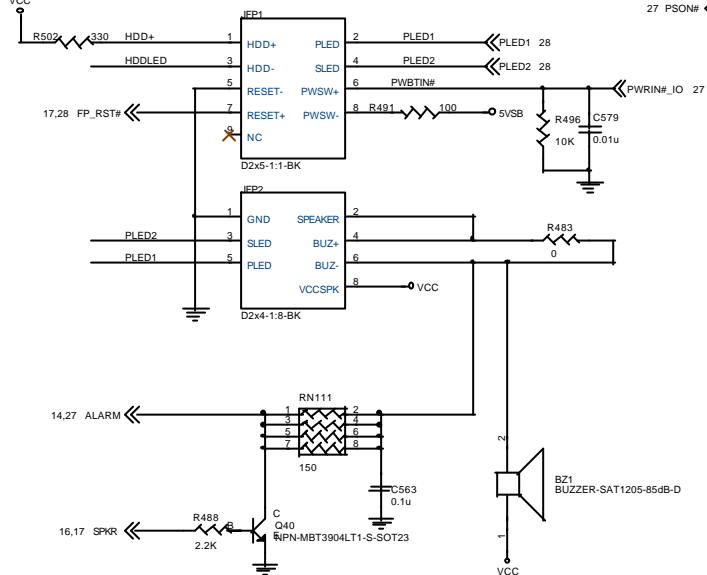


Title			
MS-6570			
Size	Document Number MS5 ACPI Controller		Rev 0A
Date	Thursday, August 01, 2002	Sheet	28 of 30

ESD Protect



For MSI / Intel Front Panel



Title		
MS-6570		
Size	Document Number	Rev
	Front Panel & ATX Power	0A
Date	Thursday, August 01, 2002	Sheet 28 of 30

DATE	DESCRIPTION
4/16	1. First version initiated.

DATE	DESCRIPTION

DATE	DESCRIPTION
7/5 Rev.0B	Changed HSDIN#[0..1] form pull_down to pull_up Voore
	Added J10 for user/safe mode selection
	Changed R203/R207 from pull_down to pull_up
	Added R507 where connected to VCCA_PLL
	Used VCCPLL_NB to control PWROK_SB delay
	Added pull_up resistor R526/R527 for PERR#/SERR# of AGP slot
	Swap APICD[0..1] for correct connection
	Added comm chock for USB 2.0
	IEEE1394 power circuit modified

Title		
MS-6570		
Size	Document Number	Rev
	History	0A
Date: Thursday, August 01, 2002 1 Sheet 30 of 30		