[FCN20221116O1]

Confidential

PM9A1 FW Change Notification

2022. Nov

Memory Business, Quality Assurance Division

SAMSUNG

Contents

Background

- **Purpose : Samsung PM9A1 NVMe SSD F/W Change to 78 version**

- **Reason of change**
  - Fix side effect of 77version FW (* Samsung officially informed to hold 77ver)

- **Samsung internal schedule**
  - Samsung internal Qualification : Nov-16th-2022
  - Release schedule : : Nov-16th-2022

PM9A1 P/N & New FW information

Product	Density	Samsung P/N	Current Firmware	Hold Firmware	New Firmware
M.2 (SED)	256GB	MZVL2256HCHQ-00B07	GXA7602Q	GXA7702Q	GXA7802Q
	512G	MZVL2512HCJQ-00B07			
	1TB	MZVL21T0HCLR-00B07			
	2TB	MZVL22T0HBLB-00B07	GXB7602Q	GXB7702Q	GXB7802Q
M.2 (non SED)	256GB	MZVL2256HCHQ-00A00	GXA7601Q	GXA7701Q	GXA7801Q
		MZVL2256HCHQ-00B00			
	512G	MZVL2512HCJQ-00A00			
		MZVL2512HCJQ-00B00			
	1TB	MZVL21T0HCLR-00A00			
		MZVL21T0HCLR-00B00			
	2TB	MZVL22T0HBLB-00A00	GXB7601Q	GXB7701Q	GXB7801Q
		MZVL22T0HBLB-00B00			

FW Change List (ver.77 → ver.78)

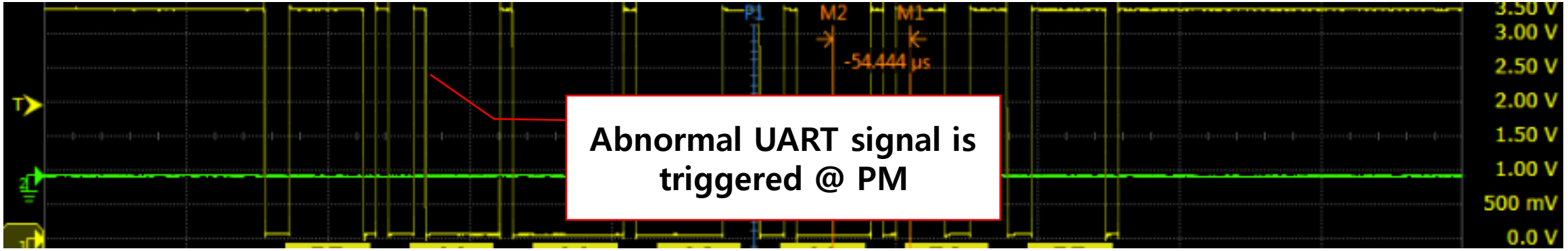
FW change List (From ver.77 to ver.78)

- Samsung would like to improve FW Quality through FW Change notification.

No.	Item	Change item	Risk Assessment
1	Fix FW for power consumption issue	- Fix for side effect of 77 FW item#1 which is 'Improve FA debug feature: Support UART feature'. After PM, device internally woke up and send UART signal, and this increased power consumption.	Middle
2	Fix FW for read performance fluctuation on CDM	- Related on 77rev FW change item#4, re-arranging block list should be done with optimized read level setting parallel. (Need to re-arrange block list to make the block list be correct). During this re-arranging operation, there is FW bug which is wrongly calculate of list size, and this FW bug caused to set wrong NAND read level.	Low

(1st item) Detailed of Change

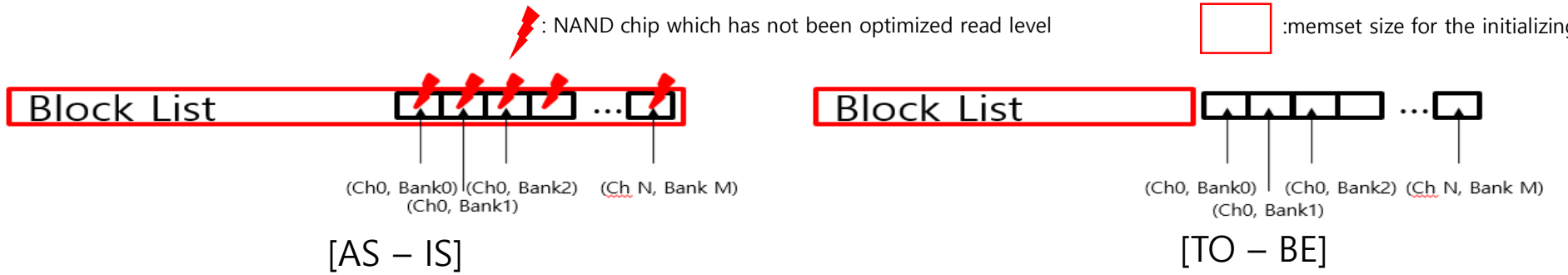
- **Issue: High power consumption observed at Modern Standby**
- **Root cause**
  - It is verified to be side effect of 77 FW item which is 'Improve FA debug feature: Support UART feature'
  - While trying to enter power mode, FW mis-knew as if host UART command is triggered and stopped to enter power mode, and this increased power consumption



- **Corrective Action**
  - Fix the wrong setting for FW mis-knew

(2st item) Detailed of Change

- **Issue : Read Performance fluctuation @ CDM**
- **Root-cause : Read Level optimization step can be skipped from side-effect of fixing #4 @77FW**
- **Failure scenario**
  - The re-arranging block list should be done during optimized read level setting parallel.
  - During Read level optimizing, in the process of initializing the list by using memset, due to a list size calculation error, the read level related FW meta information is corrupted.
  - So the NAND chip which has not been optimized read level is considered as the one which is already optimized read level.
  - Therefore, the read performance drop happened because when the block which has not been optimized read level is used and it causes protection code looping execution.
- **Corrective Action**
  - To fix error code - memset size



[AS – IS]

[TO – BE]

FW Change List (ver.76 → ver.77)

FW change List

- Samsung would like to improve FW Quality through FW Change notification.

No.	Item	Change item	Risk Assessment
1	Improve FA debug feature	- Support UART feature - Adding debug logging feature	Low
2	added FW W/A to improve AFC circuit malfunction of CTRL	- Add 2 times AFC circuit retry code when AFC circuit work abnormally If AFC circuit work abnormally, the FW initializes AFC circuit after 10ms and 15ms	Low
3	Optimized Unmap range	- # of LPN per Unmap Range needs change : Total # of LPN per Device (GXA7402Q) -> 1000 (GXA7602Q) -> 10000 (GXA7702Q)	Low
4	Fix FW - SLC compaction victim block	- When exit PM(power management mode), FW only check whether the F/G SSB Compaction Victim exists and do not remove it from the list(Fixed FW)	Low
5	Fixed LTR Latency value Register Structure	(Device internal) Register Mapping of FW Header is fixed. - It is affected to below Message TLP. Register mapping related to Snoop/No-snoop latency of device FW Header was reversed. - [R←][Msg][LTR][Snoop : --][No-snoop : --]	Low

(1st item) Detailed of Change

- **Purpose: More debug features and save to NAND in case of POR**
  - To enhance Debug feature to get more information
    - Command history/ Event ,interrupt log
    - Add debug log to have rich contents for FA
- **To save the failure information to NAND (for retrieving the logs from NAND even POR case)**
  - Customer VOC: The retention of dump log on the SSD after power down (e.g. system shutdown after SSD failure)

Category	Item	Detail	Remark
PCIe Link failure	HCORE	NVME Feature Context	- PCIe Error count - Interrupt log - Event log - Exception log - Host Command history - SQ/CS Head/Tail Doorbell - Link Down history - NAND information
		Event Logger	
	PCIe SFR	PCIe SFR	
	Event Data	PCIe Trace Buffer	
	NVMe SFR	Host Command Info	
		Controller Register Info	
		Submission/Completion Q SFR	
NAND failure	Debug Level	Program order	
		Host/ Interval	
		Get Feature	
		Status Read Info	

※ SFR : Special Function Register

(2nd item) Detailed of Change

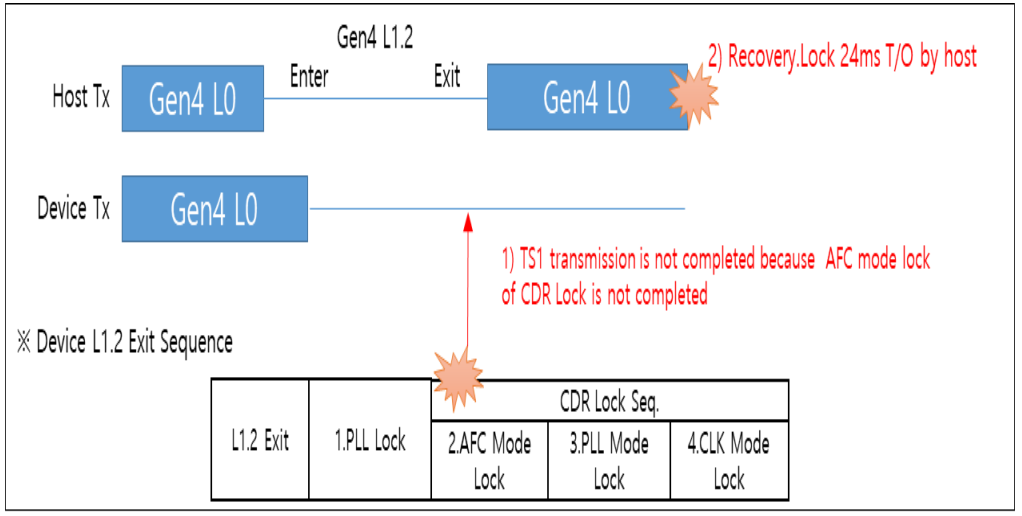
Issue

- Found Recovery.Lock 24ms Timeout when exit L1.2 during Modern standby testing

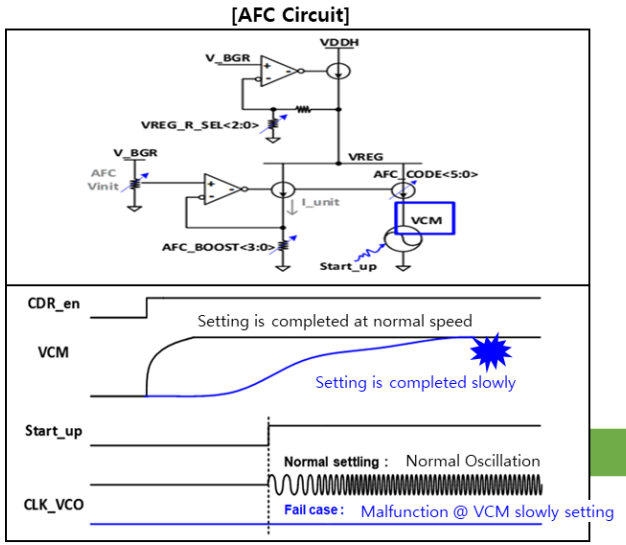
Root cause (failure mechanism)

- Device couldn't send TS1 (training Sequence 1) to Host and finally Recovery.Lock 24ms Timeout occurred and Link down happened
- When exit L1.2, CDR (Clock and Data Recovery) Lock of CTRL is not properly completed [Fig 1]
- The slow completion of VCM(Reference voltage of VCO in AFC circuit) settling was observed with very low probability during the AFC Sequence
- VCO(Clock oscillation circuit) malfunctioned due to the slow completion of VCM settling at fail samples

[Fig 1]



[Fig 2]



[Fail Mechanism]

1) SSD exit L1.2

2) VCM settling slowly during AFC @ Fail samples

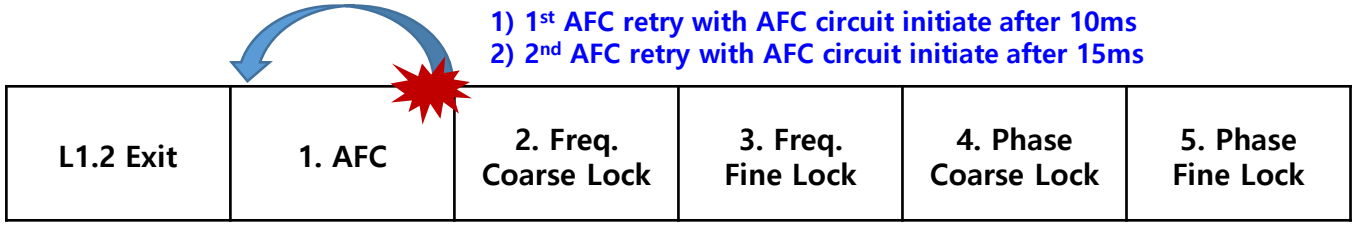
3) VCO oscillator malfunctioned due to VCM settling

4) Can not meet target Frequency during AFC

Corrective action

- Improvement Action
  - Team added W/A point to improve AFC circuit malfunction
    - ✓ Add 2 times AFC circuit retry code when AFC circuit work abnormally

    So, If AFC circuit work abnormally, the FW initializes AFC circuit after 10ms and 15ms



[AFC Retry code – 2 times]

(3rd item) Detailed of Change

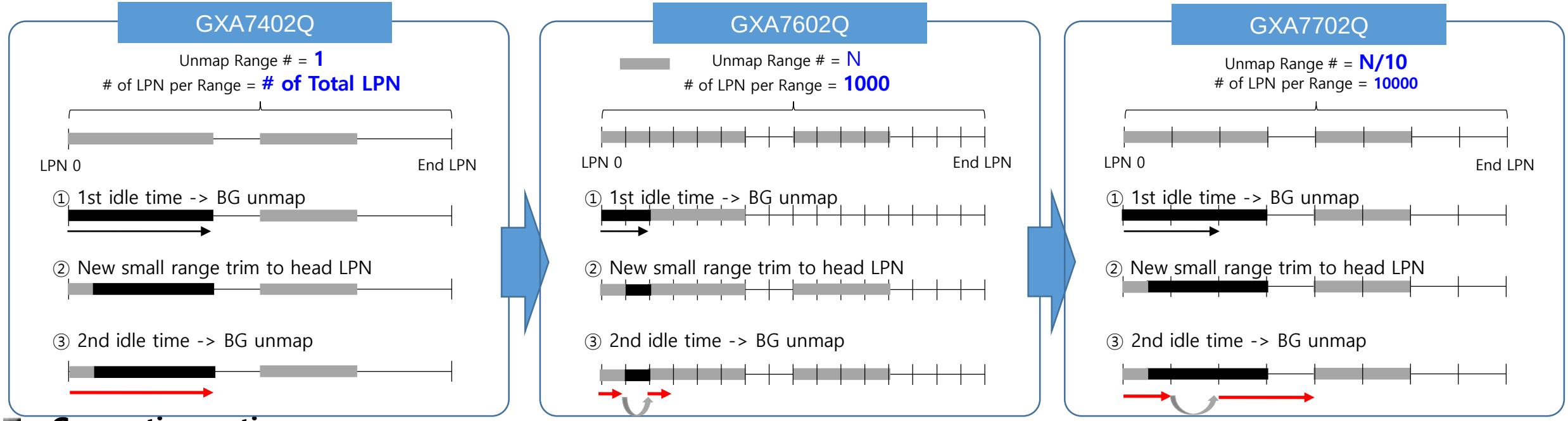
Issue

- SW encryption time takes so long

Root cause

- It is related to side effect from previous Change item(Unmap process optimization)
- Splitting # of LPN per Unmap Range was essential to guarantee to enter PM, but # was excessively small @ GXA7602Q
- FW handling time for Unmap are lengthened ➔ Free Blocks are generated more slowly

  → Ratio of unnecessary Migration & TLC write is increased



Corrective action

- # of LPN per Unmap Range needs change : Total # of LPN per Device (GXA7402Q) -> 1000 (GXA7602Q) -> 10000 (GXA7702Q)

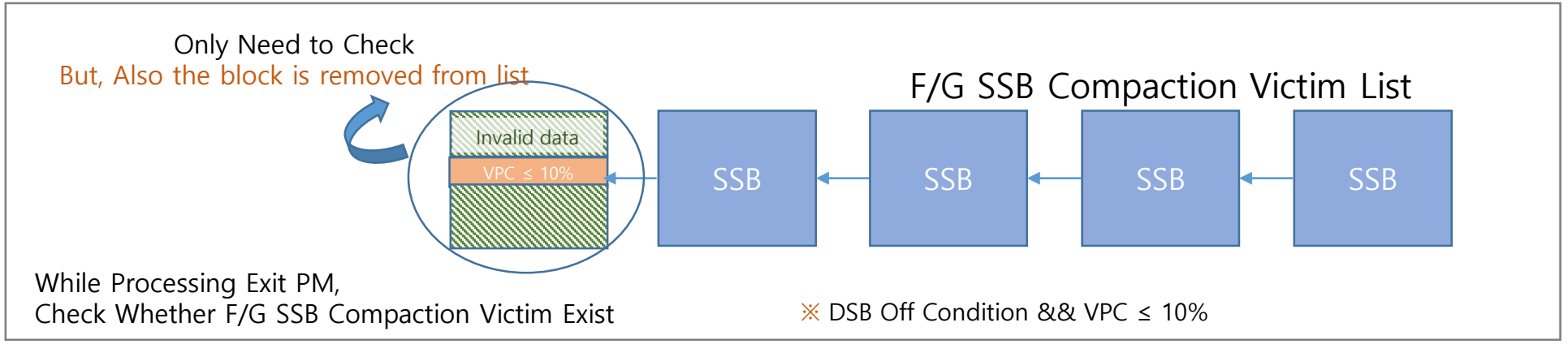
(4rd item) Detailed of Change

Issue

- Seq Write performance was dropped after long idle

Root cause

- In DSB Off state, Foreground SSB Compaction(a kind of garbage collection) is executed to receive all write data from CDM to SSB as SLC area.
- FW checks the existence of the target block for F/G SSB Compaction in the process of checking whether there is a target SSB to perform F/G SSB Compaction after Exit PM – (Select list for Victim block)
- But FW removed the target block checked from the Compaction Victim List.
- SSB Free block cannot be created because the target block is not selected as Victim of F/G SSB Compaction,
- Finally, TLC write occurred because SSB doesn't have a room for write during CDM and Seq write performance showed TLC performance



Corrective action

- When exit PM(power management mode), FW only check whether the F/G SSB Compaction Victim exists and do not remove it from the list.

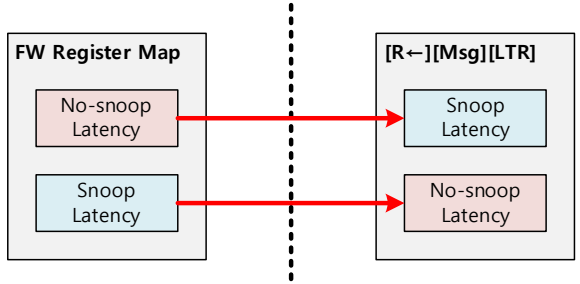
(5th item) Detailed of Change

Issue

- LTR Latency value Register was reversed

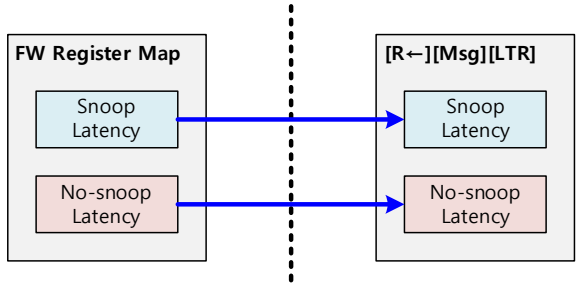
Root cause

- Register mapping related to Snoop/No-snoop latency of device FW Header was reversed.



Corrective action

- Header file of Device FW is fixed.



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